



Flaircomm Microelectronics, Inc.

FLC-BTM201

Datasheet

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CONTENTS

1. INTRODUCTION.....	6
1.1 BLOCK DIAGRAM.....	6
1.2 FEATURES.....	7
1.3 APPLICATIONS	9
2. GENERAL SPECIFICATION.....	10
3. PIN DEFINITION.....	11
3.1 PIN CONFIGURATION.....	11
3.2 PIN DEFINITION.....	11
4. BLUETOOTH MODEM	14
4.1 RF TRACE.....	14
4.2 RF RECEIVER.....	14
4.2.1 RSSI	14
4.3 RF TRANSMITTER.....	14
4.3.1 Power Amplifier	14
4.4 BASEBAND.....	14
4.4.1 Physical Layer Hardware Engine	14
5. OPERATING MODES.....	15
5.1 ACTIVE MODE.....	15
5.2 RADIO-ON MODE	15
5.3 DEEP SLEEP: 16 KB DATA RAM AND 64 KB RAM RETENTION MODE.....	15
5.4 DEEP SLEEP: 16 KB DATA RAM RETENTION MODE	15
5.5 DEEP SLEEP: NO RAM RETENTION AND EXTERNAL INTERRUPTS AND TIMER ENABLED MODE	16
5.6 DEEP SLEEP: NO RAM RETENTION AND EXTERNAL INTERRUPTS ENABLED MODE	16
6. MICROCONTROLLER, MEMORY AND BASEBAND LOGIC	17
6.1 MICROCONTROLLER.....	17
6.2 MEMORY	17
6.2.1 RAM Code and Data (Internal).....	18
6.2.2 ROM (Internal).....	18
6.2.3 OTP (Internal).....	18
6.2.4 MTP (Internal)	19
6.2.5 Flash (Internal)	19
7. PERIPHERAL INTERFACES.....	20
7.1 I2C MASTER/SLAVE (GENERAL)	20
7.2 SPI MASTER/SLAVE (GENERAL).....	21
7.3 SPI DEBUG INTERFACE.....	21
7.3.1 Instruction Cycle.....	22
7.3.2 Multi-slave Operation	22
7.4 UART (GENERAL)	22
7.4.1 UART Configuration Settings.....	23
7.4.2 UART Configuration While In Deep Sleep	23
7.5 PWMS.....	23
7.5.1 3D Shutter Control PWM.....	23
7.5.2 LED Control PWM.....	24
7.6 LCD GLASS DRIVER	24
7.7 KEY SCANNER	24
7.8 QUADRATURE DECODERS	25
7.9 INFRARED OUTPUT.....	26

7.10	AUDIO	26
7.10.1	Digital Microphone.....	26
7.10.2	G.722 Codec	26
7.11	10-BIT AUX ADC	27
8.	AUXILIARY FEATURES	28
8.1	BATTERY MONITOR.....	28
8.2	TEMPERATURE SENSOR.....	28
9.	PROGRAMMABLE I/O PORTS, PIO AND AIO.....	29
9.1	GENERAL PIOS	29
9.2	AIOS	29
9.3	DIGITAL PIN STATES ON INITIAL POWER UP	29
9.4	LCD GLASS MID-RAIL DRIVE	29
9.5	ANALOGUE PROPERTIES OF THE PIO	30
9.6	PIO CONFIGURATION OPTIONS.....	30
10.	BTM201 SOFTWARE STACK.....	31
11.	POWER	32
11.1	RESET.....	32
12.	ELECTRICAL CHARACTERISTICS	33
12.1	ABSOLUTE MAXIMUM RATINGS	33
12.2	RECOMMENDED OPERATING CONDITIONS	33
12.3	INPUT/OUTPUT TERMINAL CHARACTERISTICS.....	33
12.3.1	Digital I/O Terminals.....	33
12.3.2	AIO	34
12.4	ESD PROTECTION	34
13.	CURRENT CONSUMPTION.....	35
14.	REFERENCE DESIGN.....	36
15.	MECHANICAL CHARACTERISTICS.....	37
16.	RECOMMENDED REFLOW PROFILE	38
17.	ORDERING INFORMATION.....	40
17.1	PRODUCT PACKAGING INFORMATION	40
17.2	ORDERING INFORMATION.....	42
17.2.1	Product Revision	42
17.2.2	Shipping Package	42
17.2.3	Product Package.....	42
17.2.4	Product Grade	43

TABLES AND FIGURES

Figure 1: Block Diagram of BTM201	6
Figure 2: Pin Configuration (BTM201).....	11
Figure 3: Baseband Digits Block Diagram	17
Figure 4: Peripheral Interfaces Block Diagram	20
Figure 5: SPI Timing Diagram	21
Figure 6: Example Keyboard Matrix 3x2 Size.....	25
Figure 7: BTM201 Audio.....	26
Figure 8: 10-bit Aux ADC Reference.....	27
Figure 9: Software Architecture	31
Figure 10: Reference Design (BTM201)	36
Figure 11: Mechanical Characteristics (BTM201)	37
Figure 12: Recommended Reflow Profile	38
Figure 13: Product Packaging Information (Plastic Tray).....	40
Figure 14: Product Packaging Information (Tape).....	41
Figure 15: Ordering Information	42
Table 1: General Specification	10
Table 2: Pin Definition.....	13
Table 3: Instruction Cycle for an SPI Transaction	22
Table 4: UART Signals	22
Table 5: UART Configuration Settings	23
Table 6: Pin States on Initial Power Up	29
Table 7: BTM201 PIO Configuration Options	30
Table 8: BTM201 Absolute Maximum Ratings	33
Table 9: BTM201 Recommended Operating Conditions.....	33
Table 10: BTM201 Input Voltage Levels.....	33
Table 11: BTM201 Output Voltage Levels.....	33
Table 12: BTM201 Input and Tristate.....	34
Table 13: BTM201 Input and Tristate (Continued)	34
Table 14: BTM201 AIO.....	34
Table 15: BTM201 10-bit Aux ADC	34
Table 16: BTM201 ESD Handling Ratings	34
Table 17: Current Consumption.....	35
Table 18: Product Revision.....	42
Table 19: Shipping Package.....	42
Table 20: Product Package.....	42
Table 21: Product Grade	43

1. Introduction

FLC-BTM201 is a Bluetooth low energy (BLE) module supporting BT4.2 (BLE only). This module enables customers to add ultra-low power wireless connectivity to their products. The module provides everything required to create a Bluetooth low energy product with RF, base band, MCU, system clock, antenna and qualified Bluetooth 4.2 (BLE only) stack and customer application settings. It also enables the transfer of short data sets between compact devices opening up a completely new area of Bluetooth applications such as watches, TV remote controls, medical sensors and fitness trainers.

1.1 Block Diagram

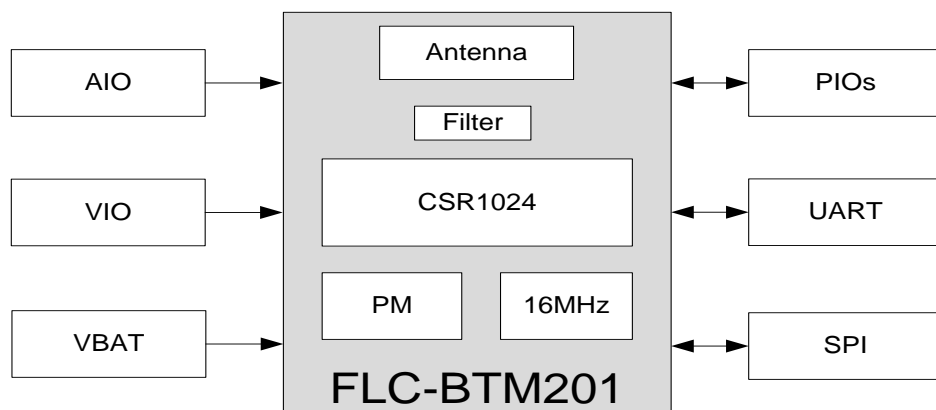


Figure 1: Block Diagram of BTM201

1.2 Features

Ultra Low Power Bluetooth low energy technology Radio

- Module with antenna and bandpass filter
- Bluetooth v4.2 specification compliant

Bluetooth Transmitter

- 2 dBm RF transmit power
- TX power control

Bluetooth Receiver

- -90 dBm sensitivity
- -91.5 dBm RX Boost mode available: Enhances RX sensitivity at higher receive current
- Digital demodulator for improved sensitivity and co-channel rejection
- Fast AGC for enhanced dynamic range

Bluetooth Stack

Protocol stack runs on the integrated MCU:

- Support for Bluetooth v4.2 specification features:
 - Master and slave operation
 - Including encryption
- Software stack in firmware includes:
 - GAP
 - L2CAP
 - Security manager
 - Generic attribute protocol
 - Attribute profile
 - Bluetooth low energy technology profile support

Baseband and Software

- Integrated MAC for all packet types enables packet handling without the need to involve the MCU

Audio

- Digital microphone input
- I²S port for PCM I/O
- G.722 Codec

Physical Interfaces

- 15 digital flexible PIOs
- 1 analogue AIO
- UART
- SPI master interface
- Debug SPI interface for programming
- I²C master controller
- 4 x quadrature decoders
- PWM 3D shutter control
- 5 x LED PWMs
- Keyboard scanner
- LCD glass drive
- 10-bit Aux ADC
- IR encoder

Auxiliary Features

- Battery monitor
- 6 power modes
- Power management features include software shutdown and hardware wake-up
- Wake-up power management from any PIO
- Integrated switch-mode power supply
- Linear regulator (internal use only)
- AES-128
- Watchdog timer

Memory

- 256 KB internal flash
- 64 KB (Code) and 16 KB (Data) RAM
- 192 KB ROM
- 60 KB OTP
- 256 Byte MTP

Battery

- Battery input voltage 3.6 V to 1.4 V

Temperature Specification

- Operating temperature -30 to 85 °C

1.3 Applications

- Bluetooth low energy technology:
 - HID: keyboards, mice, touchpads, advanced remote controls with voice activation
 - Sports and fitness sensors: heart rate, runner/cycle speed and cadence
 - Health sensors: blood pressure, thermometer and glucose meters
 - Mobile accessories: watches, proximity tags, alert tags and camera controls
 - Smart home: heating/lighting control
- CSRmesh™ connectivity: Internet of Things control

2. General Specification

Bluetooth Specification	
Standard	Bluetooth4.2(BLE only)
Frequency Band	2.402GHz ~ 2.480GHz
Antenna	Yes
Clock	16MHz
Interface	UART, I2C, PIO, SPI, AIO
Sensitivity	-90dBm@0.1%BER
RF TX Power	2dBm
Power	
Supply Voltage	1.4 ~ 3.6V DC
Operational Current	Refer to Table 17
Deep Sleep Current	Refer to Table 17
Operating Environment	
Temperature	-30°C to +85°C
Certifications	TBD
Environmental	RoHS Compliant
Dimension and Weight	
Dimension	18mm x 10.6mm x 2.7mm
Weight	TBD

Table 1: General Specification

3. Pin Definition

3.1 Pin Configuration

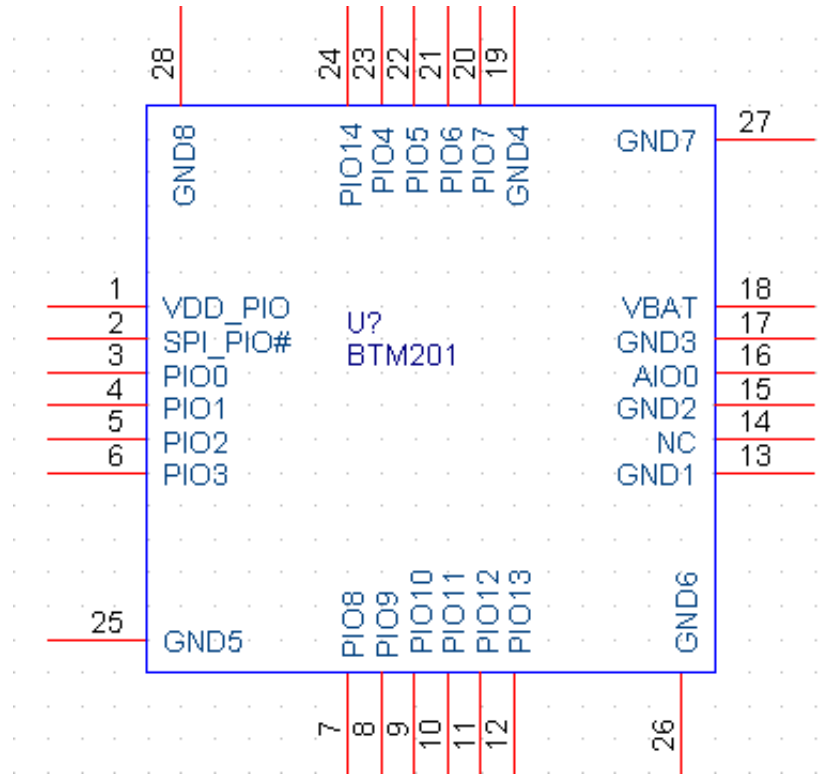


Figure 2: Pin Configuration (BTM201)

3.2 Pin Definition

Pin	Symbol	Pin Type	Description
1	VDD_PIO	Power supply	Positive supply for digital I/O ports PIO[14:0] and SPI_PIO#
2	SPI_PIO#	Input with strong internal pull-down	Selects Debug SPI on PIO[3:0].
3	PIO0	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 0
4	PIO1	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 1

5	PIO2	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 2
6	PIO3	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 3
7	PIO8	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 8
8	PIO9	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 9
9	PIO10	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 10
10	PIO11	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 11
11	PIO12	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 12
12	PIO13	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 13
13	GND1	GND	GND
14	NC	Not used	Not used
15	GND2	GND	GND
16	AIO0	Unidirectional analogue	Analogue programmable input line
17	GND3	GND	GND

18	VBAT	Power supply	Positive supply from the battery.
19	GND4	GND	GND
20	PIO7	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 7
21	PIO6	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 6
22	PIO5	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 5
23	PIO4	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 4
24	PIO14	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 14
25	GND5	GND	GND
26	GND6	GND	GND
27	GND7	GND	GND
28	GND8	GND	GND

Table 2: Pin Definition

4. Bluetooth Modem

BTM201's modem supports Bluetooth low energy technology and has 4 link controller blocks supporting up to 4 connections.

4.1 RF Trace

BTM201 contains an antenna and a bandpass filter.

4.2 RF Receiver

The receiver features a near-zero IF architecture enabling the channel filters to be integrated onto the die. Sufficient out-of-band blocking provided on die at the LNA input enables the receiver to be used in close proximity to GSM and W-CDMA cellular phone transmitters without being significantly desensitised:

- Receive sensitivity is typically -90 dBm
- Software selectable Boost mode can be enabled for additional sensitivity
- An ADC digitises the IF received signal
- An AGC supports the Bluetooth v4.2 specification's full range of input signal levels

4.2.1 RSSI

Front-end LNA gain is changed according to measured RSSI, keeping the first mixer input signal within a limited range. This improves the dynamic range of the receiver, improving performance in interference-limited environments.

4.3 RF Transmitter

4.3.1 Power Amplifier

The internal PA can deliver a maximum of 2 dBm at the antenna. The software can be configured to deliver lower output powers to reduce the current consumption during transmit.

4.4 Baseband

4.4.1 Physical Layer Hardware Engine

Dedicated logic performs:

- Cyclic redundancy check
- Encryption
- Data whitening
- Access code correlation

5. Operating Modes

BTM201 has 6 operating modes. 4 are Deep Sleep modes:

- Active
- Radio-on
- Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention
- Deep Sleep: 16 KB Data RAM Retention
- Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled
- Deep Sleep: No RAM Retention and External Interrupts Enabled

5.1 Active Mode

In Active mode, the processor runs:

- Code and/or performs activities with peripherals.
- With at least 1 link controller powered.

5.2 Radio-on Mode

In Radio-on mode, the Bluetooth radio is turned on.

NOTE: Radio-on mode can only be entered from Active mode.

5.3 Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention Mode

In Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- BTM201 supports activity in peripherals to perform a particular operation (e.g. PWMs, keyboard scanner) or wake the chip on activity (e.g. UART, application SPI).
- Link controller state is maintained: this can be active (advertising, scanning or in a connection) and BTM201 can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power controlled using power gating.

5.4 Deep Sleep: 16 KB Data RAM Retention Mode

In Deep Sleep: 16 KB Data RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- BTM201 supports activity in peripherals to perform a particular operation (e.g. PWMs, keyboard scanner) or wake the chip on activity (e.g. UART, application SPI).
- Link controller state is maintained: this can be active (advertising, scanning or in a connection) and BTM201 can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power controlled using power gating.

5.5 Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled Mode

In Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled mode:

- VBAT must always be present.
- A PIO can wake the chip (programmable as in Deep Sleep: No RAM Retention and External Interrupts Enabled mode).
- The following can wake the chip:
 - PIO hibernate timer time-out.
 - Temperature change.
 - Low battery.

5.6 Deep Sleep: No RAM Retention and External Interrupts Enabled Mode

In Deep Sleep: No RAM Retention and External Interrupts Enabled mode:

- An attached battery can be used as a wakeup.
- No timers run, therefore BTM201 can only be woken by a PIO or a rise on VBAT.
- VBAT can be removed if VIO remains powered, because the pull states of pads are preserved.
- Ignore a rise on VBAT until a PIO has latched an event (enabling 2 different Deep Sleep: No RAM Retention and External Interrupts Enabled modes).
- The PIOs that BTM201 is sensitive to on wakeup are programmable, i.e. it is possible to ignore events on some PIOs but not others.

6. Microcontroller, Memory and Baseband Logic

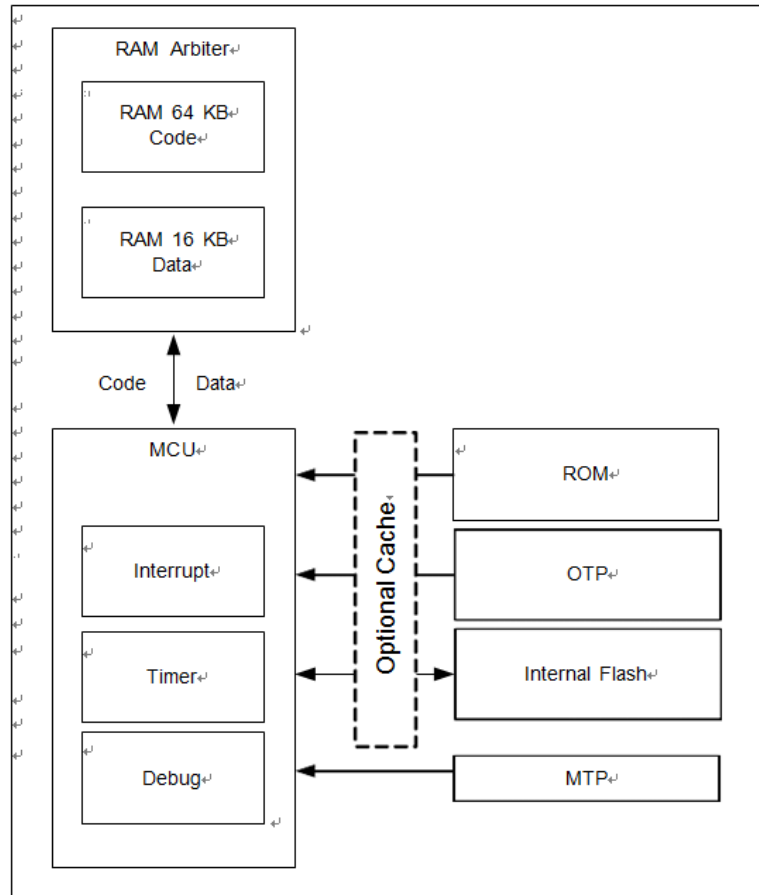


Figure 3: Baseband Digits Block Diagram

6.1 Microcontroller

The MCU, interrupt controller and event timer run the Bluetooth software stack and control the Bluetooth radio and external interfaces. A 16-bit RISC microcontroller is used for low power consumption and efficient use of memory.

6.2 Memory

BTM201 memory includes:

- RAM Code and Data (Internal)
- ROM (Internal)
- OTP (Internal)
- MTP (Internal)
- Flash (Internal)

Memory spaces include:

- Application Store: A storage area for customer applications, located in internal OTP or internal/ external SPI flash.
- Configuration Store: An area of memory used to store configuration settings (ROM, OTP, MTP, RAM, SPI flash).
- User Store: OTP (programmable once then read-only), MTP (multiple-time programmable) and SPI flash data storage available to user applications at runtime.

6.2.1 RAM Code and Data (Internal)

BTM201 has RAM for code and data.

NOTE: Either RAM is available for either code or data.

Code RAM

- 64 KB
- Primary use for developing applications for eventual storage in OTP memory
- Can be used as a cache for applications stored in flash or OTP memory
- Can be used as code or data RAM if not used as a code cache
- Software provides details of the area of shared RAM to the user application
- Part or all of the code RAM is powered down to save power when not in use

Data RAM

- 16 KB
- Primary use for firmware and applications
- The use of all data RAM for executing code is possible (although there are some restrictions on when this can be done)

6.2.2 ROM (Internal)

192 KB of internal ROM is available for system firmware implementation.

NOTE: Code executes from ROM and RAM.

6.2.3 OTP (Internal)

60 KB of OTP is available for storage of user applications:

- One-time programmable
- Enables reading and writing of information to the configuration store
- Enables downloading of software
- Has a storage provider driver
- PMU supplies power

6.2.4 MTP (Internal)

256 Bytes of MTP is an internal NVM where applications can store configuration data (for example, Bluetooth addresses and Link Keys):

- 10,000 erase/write cycles
- Multiple-time programmable

6.2.5 Flash (Internal)

256 KB of flash (internal) memory is available for user applications:

- 10,000 erase/write cycles
- Applications can be downloaded to the internal flash using OTA: An update mechanism for a remote host to download an application to the IC via a Bluetooth low energy technology link
- Internal flash is accessed at a speed lower than the processor can run: This means that application code executing from flash executes slower than that in OTP (or RAM). This can be mitigated by the use of code RAM as a cache

7. Peripheral Interfaces

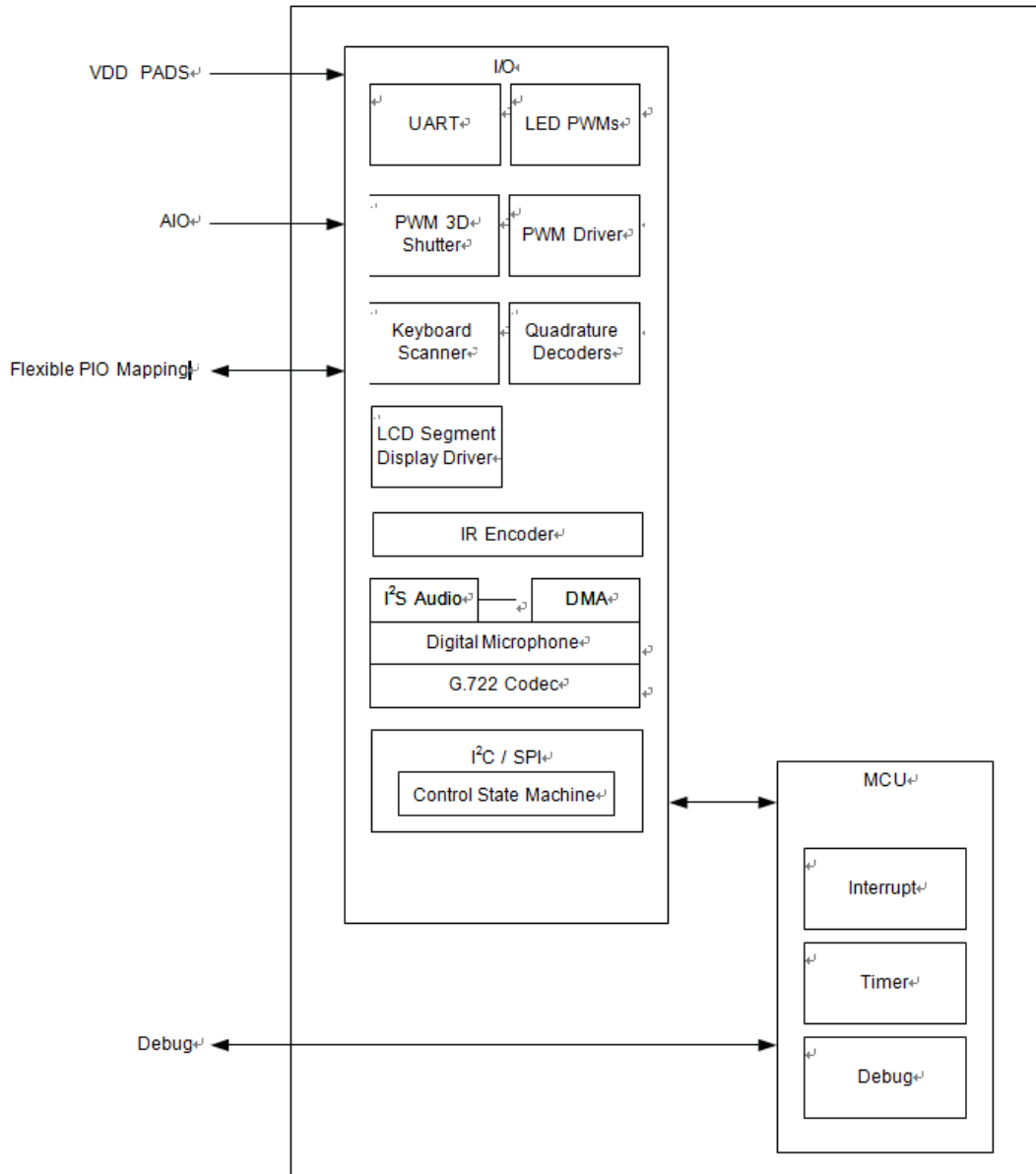


Figure 4: Peripheral Interfaces Block Diagram

7.1 I2C Master/Slave (General)

BTM201 has 1 I²C master/slave general interface for communication with external peripherals and sensors:

- Maximum clock speed 1 MHz
- Data transmitting/receiving of variable byte length
- 7-bit and 10-bit addressing modes

- Configurable:
 - PIO pins for SCL and SDA
 - I²C clock: 100 kHz default (software-configurable) at 1:1 duty-cycle (asymmetric if required)
 - Supports slave clock stretching
 - BTM201 is Fast Mode and Fast Mode+ compatible.

NOTE: Strong pull is sufficient for I²C on all PIO pads.

7.2 SPI Master/Slave (General)

BTM201 has 1 SPI master/slave general interface for communication with other devices. It supports:

- SPI master and slave
- All 4 modes supported
- 2 methods of transferring data to memory:
 - DMA to/from memory:
 - 8-bit or 16-bit word size
 - Big and little-endian
 - Software reads and writes to FIFOs: variable from 1 to 16 bits
- Interrupt callbacks to processor allow SPI as a slave to indicate that it requires service
- Deep sleep mode (depending on clock)

Figure 3 shows a simple SPI timing diagram.

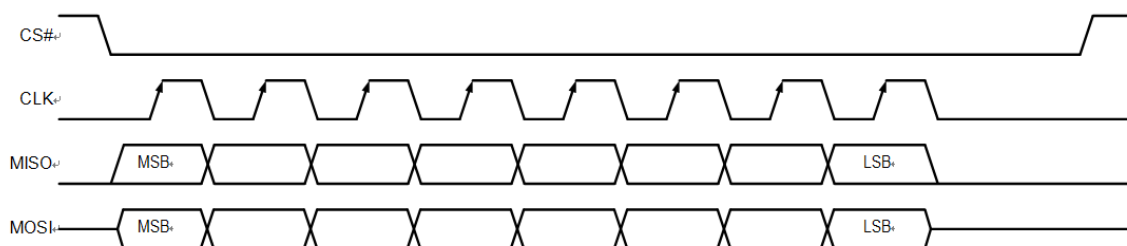


Figure 5: SPI Timing Diagram

7.3 SPI Debug Interface

NOTE: The BTM201 debug SPI interface is available in SPI slave mode to enable an external MCU to program and control the BTM201. The protocol of this interface is proprietary. A 128-bit lock key secures application code. The 4 SPI debug lines directly support this function on PIO[3:0].

The SPI programs, configures and debugs the BTM201. It is required in production.

Take SPI_PIO# high to enable the SPI debug feature on PIO[3:0].

BTM201 uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

Data is written or read one word at a time, or the auto-increment feature is available for block access.

7.3.1 Instruction Cycle

The BTM201 is the slave and receives commands on DEBUG_MOSI and outputs data on DEBUG_MISO.

Table 3 shows the instruction cycle for an SPI transaction.

1	Reset the SPI interface	Hold DEBUG_CS# high for 2 DEBUG_CLK cycles
2	Write the command word	Take DEBUG_CS# low and clock in the 8-bit command
3	Write the address	Clock in the 16-bit address word
4	Write or read data words	Clock in or out 16-bit data word(s)
5	Termination	Take DEBUG_CS# high

Table 3: Instruction Cycle for an SPI Transaction

With the exception of reset, DEBUG_CS# must be held low during the transaction. Data on DEBUG_MOSI is clocked into the BTM201 on the rising edge of the clock line DEBUG_CLK. When reading, the BTM201 replies to the master on DEBUG_MISO with the data changing on the falling edge of the DEBUG_CLK. The master provides the clock on DEBUG_CLK. The transaction is terminated by taking DEBUG_CS# high.

The auto increment operation on the BTM201 cuts down on the overhead of sending a command word and the address of a register for each read or write, especially when large amounts of data are to be transferred. The auto increment offers increased data transfer efficiency on the BTM201. To invoke auto increment, DEBUG_CS# is kept low, which auto increments the address while providing an extra 16 clock cycles for each extra word written or read.

7.3.2 Multi-slave Operation

Do not connect the BTM201 in a multi-slave arrangement by simple parallel connection of slave MISO lines. When BTM201 is deselected (DEBUG_CS# = 1), the DEBUG_MISO line does not float. Instead, BTM201 outputs 0 if the processor is running or 1 if it is stopped.

7.4 UART (General)

The BTM201 UART interface provides a simple mechanism to communicate with other serial devices using the RS232 protocol.

Table 4 lists the 4 signals that implement the UART function in BTM201.

Signal	Description
UART_RX	Pin to receive UART data from another device
UART_TX	Pin to transmit UART data to another device
UART_CTS	Pin to notify another device that BTM201 is ready to receive data (active low input)
UART_RTS	Pin to notify other device that BTM201 is ready to send data (active low output)

Table 4: UART Signals

7.4.1 7.4.1 UART Configuration Settings

UART configuration parameters, e.g. baud rate and data format, are set using BTM201 firmware.

NOTE: To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

Table 5 lists UART configuration settings for BTM201.

Parameter		Possible Values
Baud rate	Minimum	1200 baud ($\leq 2\%$ Error)
		9600 baud ($\leq 1\%$ Error)
	Maximum (XTAL)	1M baud ($\leq 1\%$ Error)
Parity		None, Odd or Even
Number of stop bits		1 or 2
Bits per byte		8

Table 5: UART Configuration Settings

7.4.2 UART Configuration While In Deep Sleep

The maximum baud rate is 2400 baud during deep sleep.

7.5 PWMs

BTM201 has 5 independently configurable PWM instances. A multipurpose PWM generator provides 3 modes:

- Normal PWM mode:
 - For motor control and general purpose PWM
- 3D Shutter mode:
 - For 3D shutter control
 - Cycle accurate
 - 16-bit resolution for all the configuration registers to be specified in clock cycles
 - New configuration applied on update register write or at a specific time (e.g. in response to radio traffic)
 - Variable offset after the reconfiguration can be applied
 - Configurable width of the external sync pulses
- LED mode:
 - For LED fading

7.5.1 3D Shutter Control PWM

BTM201 has a 3D shutter control PWM that is cycle accurate and can be used for driving 3D TV glasses. It has 16-bit resolution for all configuration registers to be specified in the clock cycles:

- Time On: For shutter on period
- Time Period: For shutter period
- Time Offset: Applied at a specific time (e.g. in response to radio traffic)

NOTE: A new configuration is applied on the TV sync pulse or controlled on the sync register write.

7.5.2 LED Control PWM

- BTM201 has 4 LED mode PWM blocks (2 x fast / 2 x slow). Each LED mode PWM has an 8-bit resolution for all configuration registers and a:
- Minimum brightness duty cycle (grouped in a 16-bit wide register)
- Maximum brightness duty cycle (grouped in a 6-bit wide register)
- Hold Minimum and Maximum time (grouped in a 16-bit wide register)
- Step (ramp) time
- Brightness configuration specified in units of typically 30 μ s assuming a 32 kHz clock
- Hold times specified in units of typically 16 ms assuming a 32 kHz clock
- Step time specified in units of typically 1 ms assuming a 32 kHz clock

NOTE: BTM201 supports immediate reconfiguration on the sync register write.

7.6 LCD Glass Driver

BTM201's LCD driver has the following features:

- Drives simple static and multiplexed LCD glass with no requirement for external components.
- Capable of controlling PIO pads to support bias modes:
 - Normal: Switching between GND and VCC
 - 1/2 bias: Switching between GND, 1/2 VCC and VCC
 - 1/3 bias: Switching between GND, 1/3 VCC, 2/3 VCC and VCC
- Up to 28 segments and 4 common (backplane) driver outputs
- Configurable to support non-multiplexed (static) and 2, 3 or 4 way multiplexed LCD glass
- Supports LCD glass with up to 112 display segments (4x the number of segment driver outputs)

NOTE: Unused segment outputs that can be disabled.

- LCD blanking support: Enables flashing of all segments at slow (typically 2 Hz) frequency
- LCD segment blinking support: Up to 2 segments can be configured to blink at slow frequency (typically 2 Hz)
- Flexible input clock pre-scaler to support required clock frequencies for different multiplexing modes and LCD glass characteristics.
- Ultra-low power operation to maintain LCD display with only low frequency clock input (typically 32 kHz)
- LCD clock output for pad drivers to increase output pad drivers when LCD output changes.
- Contrast control

7.7 Key Scanner

BTM201 has 1 key scanner for applications such as mouse and keyboard HID.

Figure 4 shows an example keyboard matrix at a size of 3 x 2 (PIO drive lines x PIO sense lines respectively).

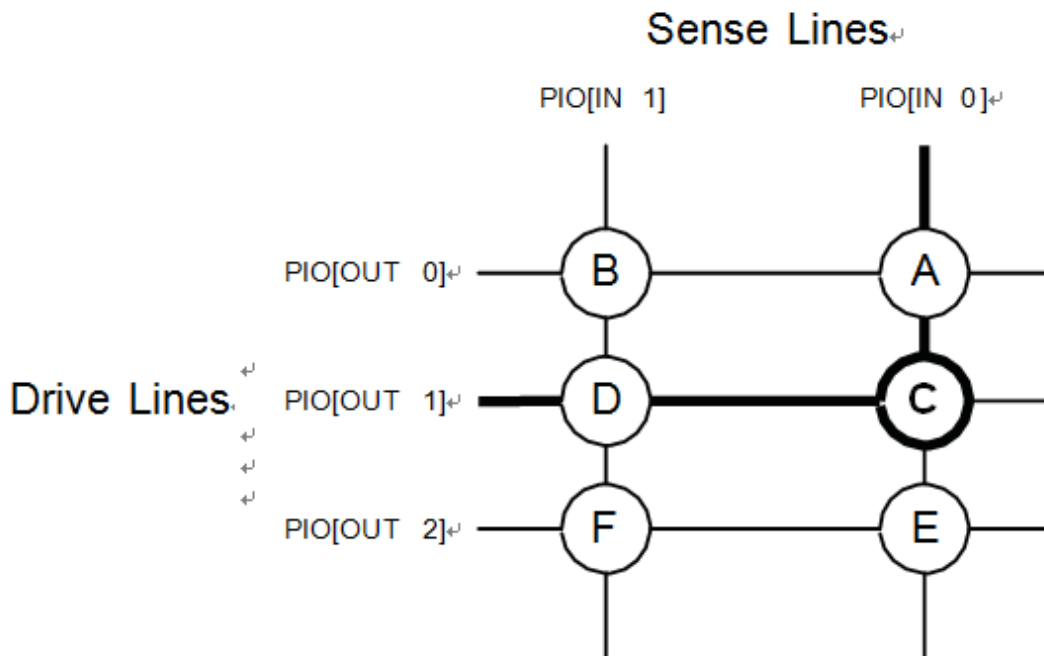


Figure 6: Example Keyboard Matrix 3x2 Size

Physical buttons are located on line crossings A to F. If a button is pressed both lines become connected. Assuming sense lines are pulled-up by internal logic, a key press, for example C can be detected by forcing PIO[OUT 1] low and reading 0 on PIO[IN 0].

It supports:

- Keypad matrix up to 12 PIO inputs (sense lines) and 18 PIO outputs (drive lines):
 - Drives 1 to 18 drive lines consecutively
 - 12-bit key registers updated every scan
- Press and release events reported to the host via callback
- Variable scan rate:
 - By default drives consecutive drive lines every clock cycle
 - Configurable number of clocks per drive line

NOTE: The key scanner does not support ghost key removal.

The key scanner configuration and control includes:

- PIO pin numbers to be used for drive and sense lines
- Scan rate, Hz and active/idle ratio
- Hardware starting and stopping
- Callback creation to receive keyboard map data.

7.8 Quadrature Decoders

- BTM201 has 4 quadrature decoders with:

- Each having a configurable simple filter on inputs (for debouncing)
- Enabling and disabling of single or multiple decoders
- Data reading functionality
- Processor interrupt generation

7.9 Infrared Output

BTM201 has 1 IR output for applications such as infrared remote control. It can run from Fast XTAL and Intermediate clocks.

7.10 Audio

Figure 7 shows BTM201 audio.

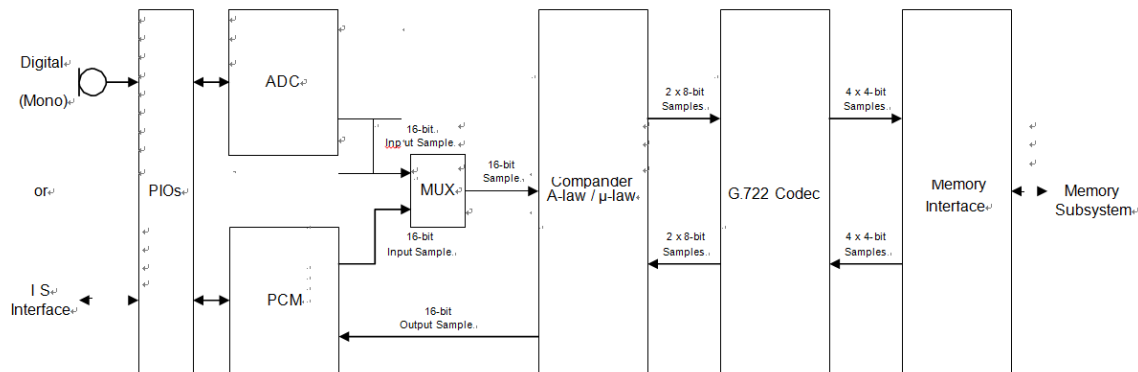


Figure 7: BTM201 Audio

NOTE: Digital microphone and I²S input cannot be active at the same time.
G.722 codec cannot encode and decode at the same time.

7.10.1 Digital Microphone

- BTM201 has 1 digital microphone input with:
- 1 or 2 Mbps sample rate
- Software selectable as left or right channel
- G.722 encoder or bypass option
- Audio routed to firmware only (not to I²S)
- Software supporting DMIC clock frequencies of 500 kHz, 1 MHz, 2 MHz, and 4 MHz

7.10.2 G.722 Codec

- BTM201 has a G.722 Codec, featuring:
- Output: 48 kbps (optional 56 or 64 kbps)
- Input: 16 kHz/16-bits (optional 8 kHz/8-bits, 8 kHz/16-bits and 16 kHz/8-bits)
- Output produces 20 Byte blocks for easy GATT streaming

NOTE: Analogue audio is not provided.

7.11 10-bit Aux ADC

BTM201 has 1 10-bit Aux ADC:

- A resistive SAR ADC
- Attached to 1 AIO pad
- The processor has access to its ADC result value after exit from Deep Sleep mode
- The ADC reference is VDD_AUX, see Figure 8.

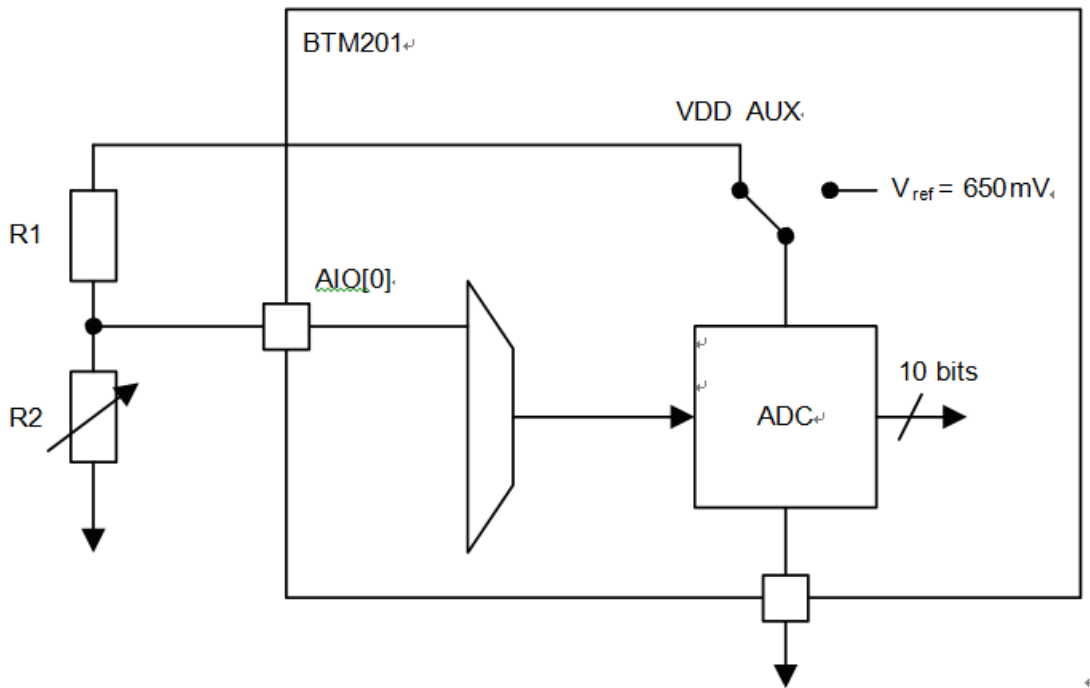


Figure 8: 10-bit Aux ADC Reference

NOTE: Figure 8 shows an additional internal 650 mV reference. This is for test purposes only. The 10-bit Aux ADC is not available during XTAL startup or battery voltage and temperature monitoring. Therefore the time to perform a conversion may be longer if the hardware is already using the ADC.

8. Auxiliary Features

8.1 Battery Monitor

BTM201 contains an internal battery monitor that reports the battery voltage to the software.

8.2 Temperature Sensor

BTM201 contains a temperature sensor that measures the temperature of the die and can report the chip temperature in °C or Kelvin using a firmware API.

9. Programmable I/O Ports, PIO and AIO

This section describes BTM201 programmable I/O ports, PIO and AIO.

9.1 General PIOs

15 lines of programmable bidirectional I/O are provided:

- May be set by the application code or used as an input or to wake the chip.
- Software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.
- At reset all lines are inputs with weak pull-down.
- Pull strength, direction and pad states preserved across all non-off states to support waking on any PIO. Configurable to wake BTM201 via an individually selectable mask for rising, falling or any edge transition from Deep Sleep modes.
- Available as interrupt request lines.
- Powered from VIO

NOTE: VIO must remain powered.

FLC cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific.

9.2 AIOS

BTM201 has 1 pin providing a unidirectional analogue programmable input line, AIO[0].

NOTE: This pin does not provide an output capability.

9.3 Digital Pin States on Initial Power Up

Table 6 shows the pin states of BTM201 on initial power up. Pull-Up and Pull-Down default to weak values unless specified otherwise.

Pin Name / Group	On Initial Power Up
SPI_PIO#	Strong Pull-Down
All other PIOs	Weak Pull-Down

Table 6: Pin States on Initial Power Up

9.4 LCD Glass Mid-rail Drive

BTM201 supports direct LCD glass driving by internally generating required voltage for one of the following modes of operation:

- 1/2 mode
- 1/3 and 2/3 mode

Voltage levels are generated and routed internally to the I/O pads configured for LCD glass driving.

NOTE: Only a single mode of operation is available.
Hardware supports up to 4 common lines and 32 segment lines.

9.5 Analogue Properties of the PIO

Most BTM201 PIOs can route in an analogue signal that can be digitised using the 10-bit Aux ADC.

NOTE: This feature may not be available in the current firmware.

9.6 PIO Configuration Options

PIO Pin	Digital Microphone	I ² S	I ² C Master Only	SPI		Debug SPI	H4 UART		Quadrature Decoder Input ^(a)		LCD		LED/PWM (b)	KeyScan		IR Encoder (Output)	GSIU					Radio		TMRCTR	
				Slave Only	Inc Master		Data	Flow	A	B	Common	Segment		Drive	Sense		TX	RX	EXT TMRCTR	ANALOG	EXT CLKOUT	RX ADC (SDDRC)	TX Data Buffer	Timer	Timer 1
PIO[14]	MIC DATA IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	y	y	COM2	y	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[13]	MIC CLK OUT	I2S WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	y	y	COM1	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[12]	MIC DATA IN	I2S CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	y	y	COM0	3	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[11]	MIC CLK OUT	I2S DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	y	y	COM3	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[10]	MIC DATA IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	y	y	COM2	y	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[9]	MIC CLK OUT	-	SDA	CLK, CS, SDA	DATA	-	RX	CTS	y	y	COM1	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[8]	MIC DATA IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	y	y	COM0	2	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[7]	MIC CLK OUT	I2S WS	SDA	CLK, CS, SDA	DATA	-	RX	CTS	y	y	COM3	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[6]	MIC DATA IN	I2S CLK	SCL	CLK, CS, SDA	DATA	-	TX	RTS	y	y	COM2	y	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[5]	MIC CLK OUT	I2S DATA	SDA	CLK, CS, SDA	DATA	-	RX	CTS	y	y	COM1	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[4]	MIC DATA IN	-	SCL	CLK, CS, SDA	DATA	-	TX	RTS	y	y	COM0	1	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[3]	MIC CLK OUT	I2S WS	SDA	CLK, CS, SDA	DATA	y	RX	CTS	y	y	COM3	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[2]	MIC DATA IN	I2S CLK	SCL	CLK, CS, SDA	DATA	y	TX	RTS	y	y	COM2	y	y	y	y	y	y	-	y	y	y	y	y	y	y
PIO[1]	MIC CLK OUT	I2S DATA	SDA	CLK, CS, SDA	DATA	y	RX	CTS	y	y	COM1	y	y	y	y	y	-	y	y	y	y	y	y	y	y
PIO[0]	-	-	SCL	CLK, CS, SDA	DATA	y	TX	RTS	y	y	COM0	0	y	y	y	y	y	-	y	y	y	y	y	y	y

Table 7: BTM201 PIO Configuration Options

Notes:

- (a) Quadrature Decoder Input A and B both require 4 PIOs to be assigned.
- (b) LED/PWM require 5 PIOs to be assigned to access all functionality.

10. BTM201 Software Stack

BTM201 is supplied with Bluetooth v4.2 specification compliant stack firmware. Figure 7 shows that the BTM201 software architecture enables the Bluetooth processing and the application program to run on the internal RISC MCU .

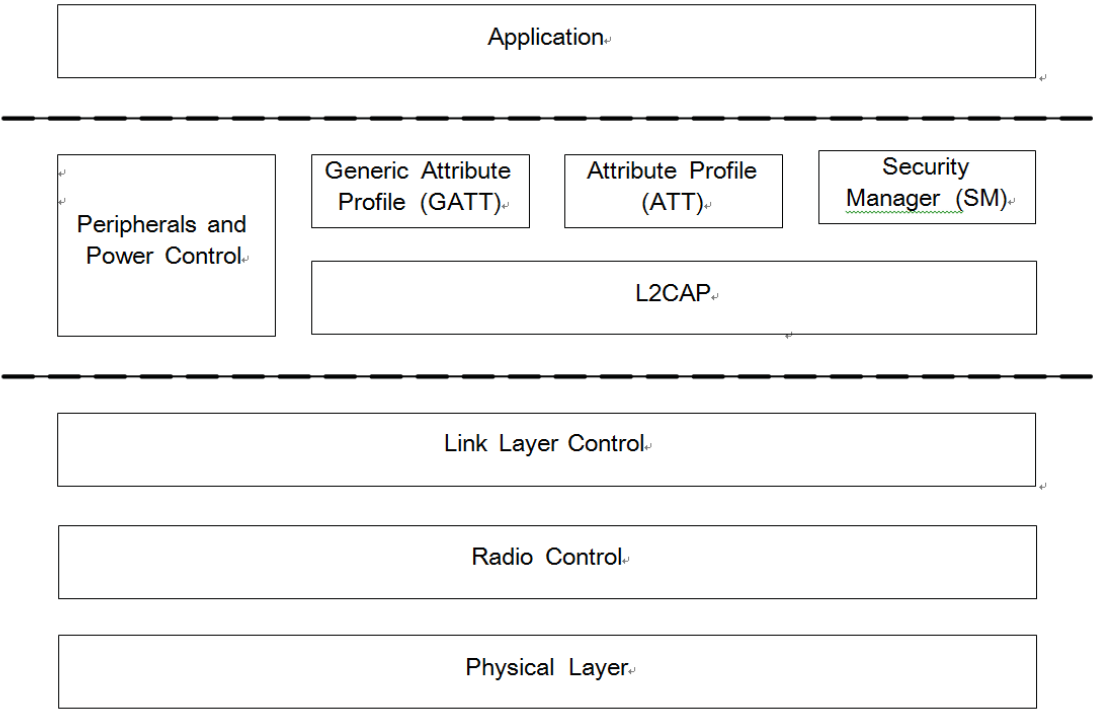


Figure 9: Software Architecture

11. Power

11.1 Reset

BTM201 is reset by:

- Power-on reset
- Software-configured watchdog timer

NOTE: VBAT input voltage must drop to 0.4 V to guarantee a rising VBAT is seen by the PMU on reassertion. VBAT takes approximately 20 s to drop to 0 V when power is removed due to circuit decoupling capacitance. To fully reset the PIO pads take all VIO pins below 0.4 V.

12. Electrical Characteristics

12.1 Absolute Maximum Ratings

NOTE: Exceeding absolute maximum ratings causes permanent damage to the BTM201.
Exposure to any absolute maximum rating for extended periods of time affects reliability.

Rating	Min	Typ	Max	Unit
Storage temperature	-40	-	85	°C
Battery (VBAT)	0	-	3.6	V
I/O supply voltage (VIO)	0	-	3.6	V

Table 8: BTM201 Absolute Maximum Ratings

12.2 Recommended Operating Conditions

Use the BTM201 recommended operating conditions to ensure optimum performance and reliability.

Operating Condition	Min	Typ	Max	Unit
Operating temperature range	-30	20	85	°C
Battery (VBAT)	1.4	3.0	3.6	V
I/O supply voltage (VIO)	1.4	3.0	3.6	V

Table 9: BTM201 Recommended Operating Conditions

12.3 Input/Output Terminal Characteristics

NOTE: Current drawn by a pin is positive (+ve), current supplied is negative (-ve).

12.3.1 Digital I/O Terminals

Input Voltage Levels	Min	Typ	Max	Unit
V _{IL} input logic level low	-	-	25% x VIO	V
V _{IH} input logic level high	75% x VIO	-	-	V

Table 10: BTM201 Input Voltage Levels

Output Voltage Levels	Min	Typ	Max	Unit
V _{OL} output logic level low, I _{OL} = 8.0 mA (Max Drive Strength)	-	-	20% x VIO	V
V _{OH} output logic level high, I _{OL} = -8.0 mA (Max Drive Strength)	80% x VIO	-	-	V
T _r /T _f (for 30 pF load)	-	-	2	ns

Table 11: BTM201 Output Voltage Levels

Input and Tristate	Min	Typ	Max	Unit
With strong pull-up	3.5	4.7	6.0	kΩ
With strong pull-down	3.5	4.7	6.0	kΩ
With weak pull-up ⁽¹⁾	8	40	50	μA

Table 12: BTM201 Input and Tristate

Input and Tristate	Min	Typ	Max	Unit
With weak pull-down ⁽¹⁾	10	40	50	μA
C _I input capacitance	-	5	-	pF

Table 13: BTM201 Input and Tristate (Continued)

NOTE: 1. Range applicable for V_{IO} between 1.8 V and 3.3 V when measured as a short circuit.

12.3.2 AIO

Input/Output Voltage Levels	Min	Typ	Max	Unit
Input voltage	0	-	1.2	V

Table 14: BTM201 AIO

12.3.2.1 10-bit Aux ADC

10-bit Aux ADC	Min	Typ	Max	Unit
Resolution	-	-	10	Bits
Input voltage range ⁽¹⁾	0	-	1.2	V
Input bandwidth	-	100	-	kHz
Conversion time	1.38	1.69	4.14	μs
Sample rate ⁽²⁾	-	-	700	Samples/s

Table 15: BTM201 10-bit Aux ADC

NOTE : 1. LSB size = 1.2V/1023.

2. The 10-bit Aux ADC is accessed through the firmware API. The sample rate given is achieved as part of this function.

12.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Table 16 shows the ESD handling maximum ratings.

Condition	Class	Max Rating
Human Body Model Contact Discharge per JEDEC EIA /JS-001-2014	1C	2 kV (all pins except RF rated at 1 kV) ⁽¹⁾
Charged Device Model Contact Discharge per JEDEC EIA	C1	500 V (all pins) ⁽¹⁾

Table 16: BTM201 ESD Handling Ratings

NOTE: 1. This value is preliminary and may be subject to change.

13. Current Consumption

Table 17 shows BTM201 total typical current consumption measured at the battery.

Mode	Description	Typical Current at 3V
Deep Sleep: No RAM Retention and External Interrupts Enabled	All functions are shut down. To wake the chip, toggle a pre-configured PIO.	1.6 μ A
Deep Sleep: No RAM Retention with External Interrupts and Timer Enabled	VIO = ON VBAT = ON	5.5 μ A
Deep Sleep: 16 KB Data RAM Retention	VIO = ON VBAT = ON RAM = ON Digital Circuits = ON SMPS = ON	10.5 μ A
Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention	VIO = ON VBAT = ON RAM = ON Digital Circuits = ON SMPS = ON	12 μ A
Idle: Shallow Sleep	VIO = ON VBAT = ON RAM = ON Digital Circuits = ON MCU = IDLE <1 μ s Wake-up Time	0.75 mA
Idle: Active	VIO = ON VBAT = ON RAM = ON Digital Circuits = ON MCU = IDLE <1 μ s Wake-up Time	1.3 mA (Execution from Cache)
		13.5 mA (Active SMEM Execution)
TX Active	2 dBm Transmit Power	5 mA Average
RX Active	-90 dBm Sensitivity	5 mA Average

Table 17: Current Consumption

14. Reference Design

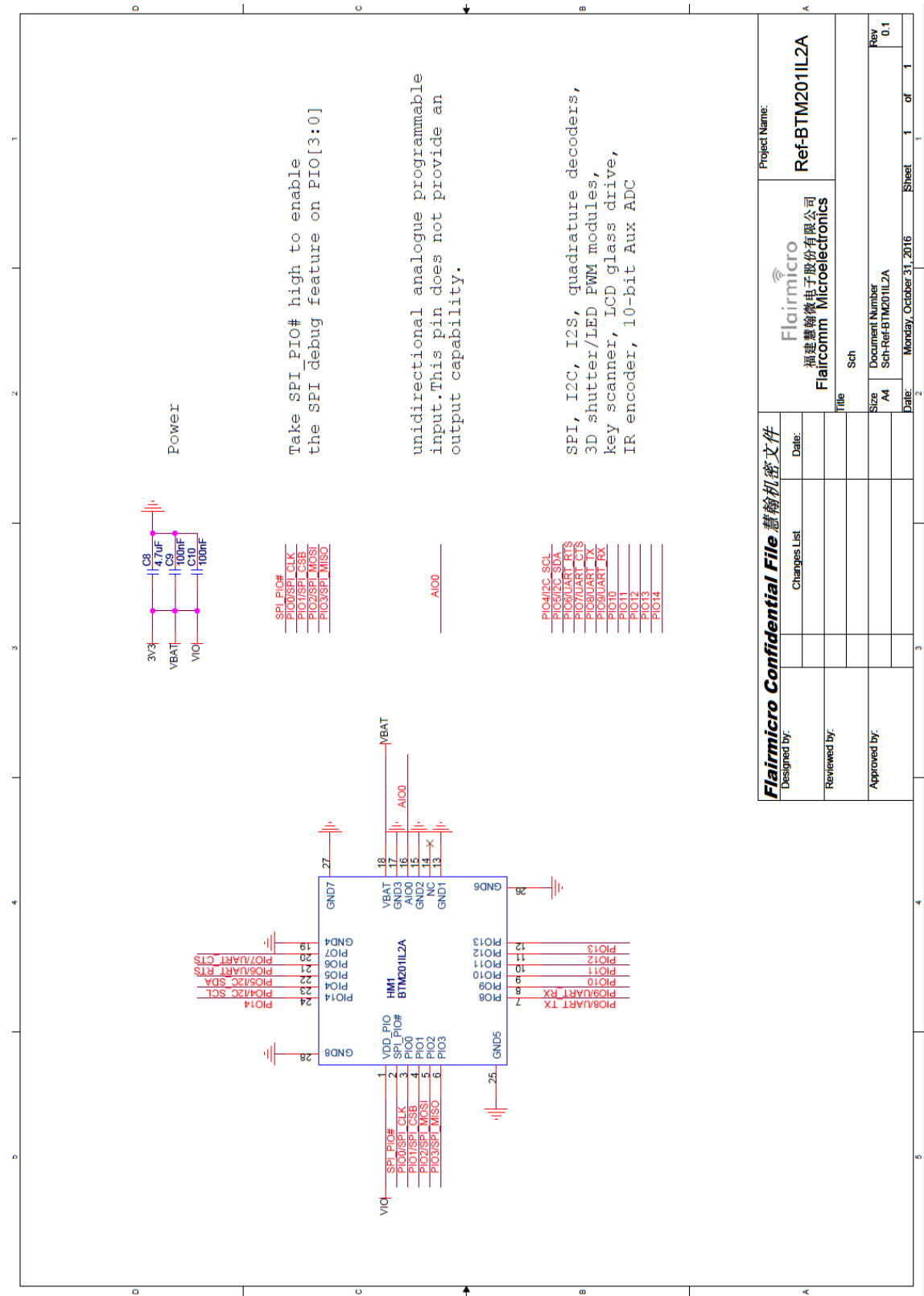


Figure 10: Reference Design (BTM201)

15. Mechanical Characteristics

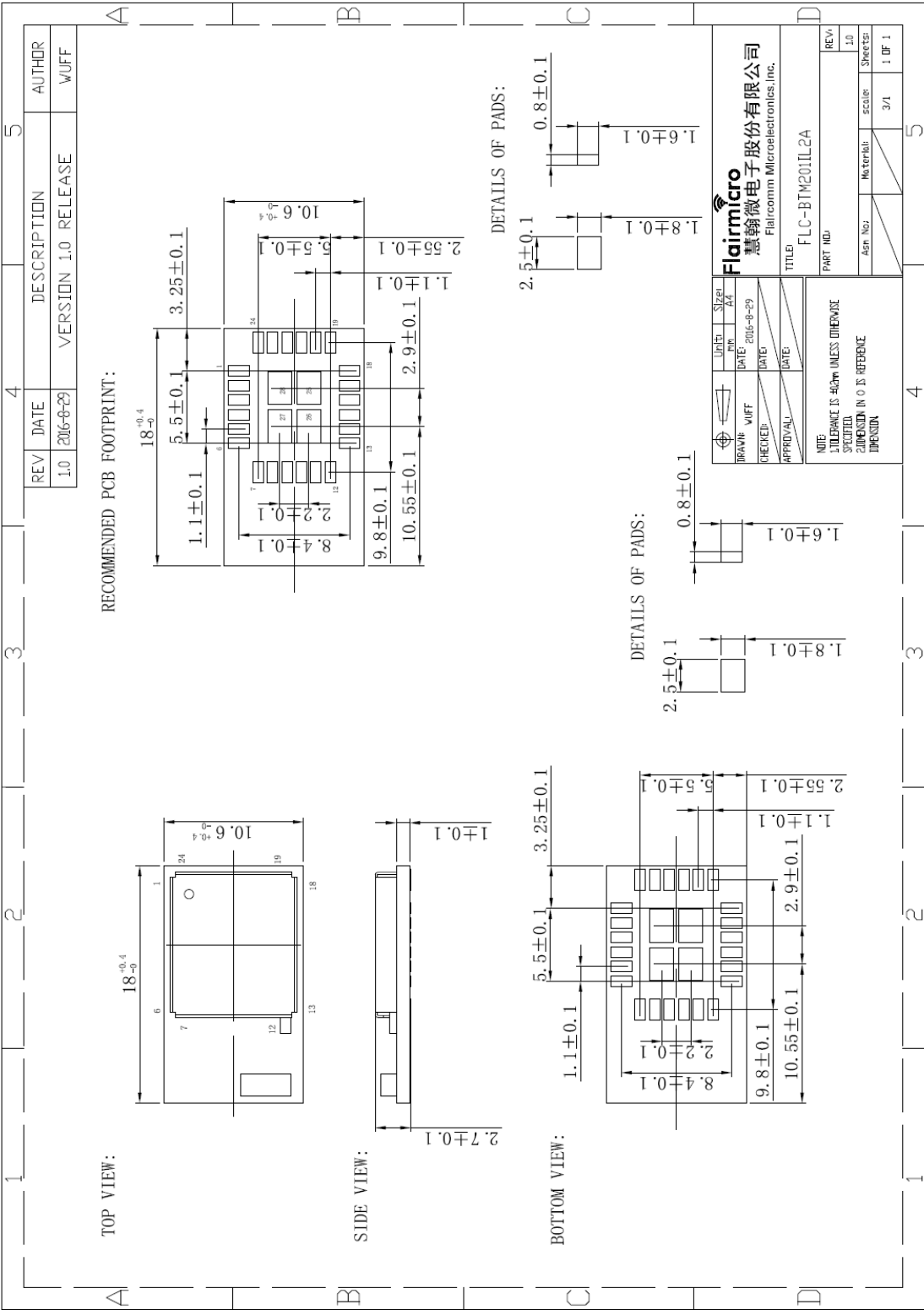


Figure 11: Mechanical Characteristics (BTM201)

16. Recommended Reflow Profile

The soldering profile depends on various parameters necessitating a set up for each application. The data here is given only for guidance on solder reflow.

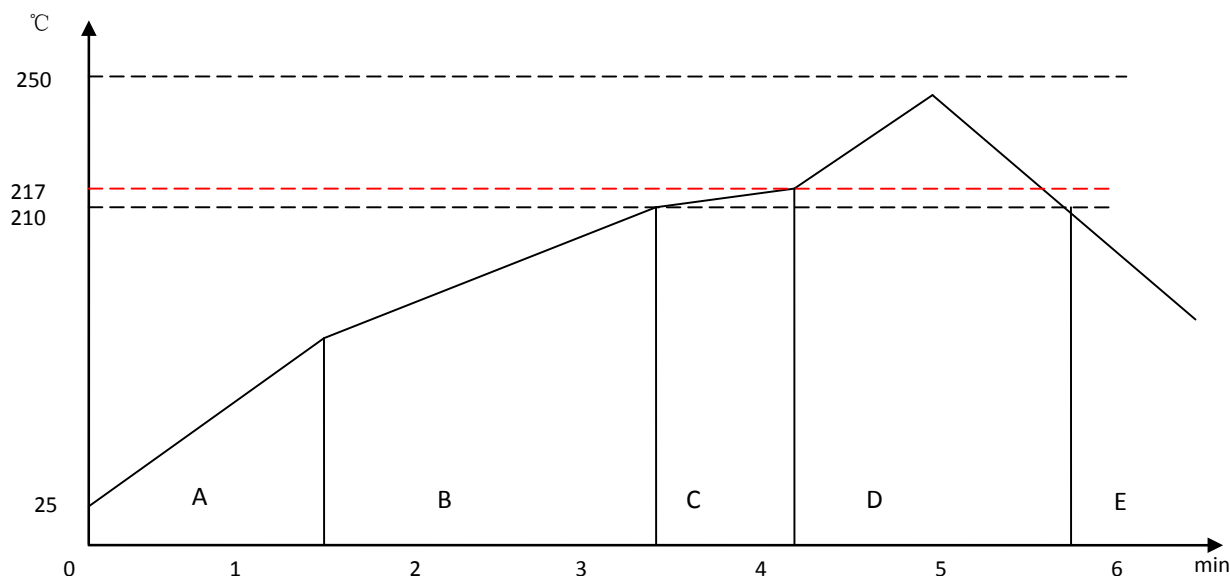


Figure 12: Recommended Reflow Profile

Pre-heat zone (A) — This zone raises the temperature at a controlled rate, **typically 0.5 – 2 °C/s**. The purpose of this zone is to preheat the PCB board and components to 120 ~ 150 °C. This stage is required to distribute the heat uniformly to the PCB board and completely remove solvent to reduce the heat shock to components.

Equilibrium Zone 1 (B) — In this stage the flux becomes soft and uniformly encapsulates solder particles and spread over PCB board, preventing them from being re-oxidized. Also with elevation of temperature and liquefaction of flux, each activator and rosin get activated and start eliminating oxide film formed on the surface of each solder particle and PCB board. **The temperature is recommended to be 150° to 210° for 60 to 120 second for this zone.**

Equilibrium Zone 2 (c) (optional) — In order to resolve the upright component issue, it is recommended to keep the temperature in 210 – 217 ° for about 20 to 30 second.

Reflow Zone (D) —The profile in the figure is designed for Sn/Ag3.0/Cu0.5. It can be a reference for other lead-free solder. The peak temperature should be high enough to achieve good wetting but not so high as to cause component discoloration or damage. Excessive soldering time can lead to intermetallic growth which can result in a brittle joint.

The recommended peak temperature (T_p) is 230 ~ 250 °C. The soldering time should be 30 to 90 second when the temperature is above 217 °C.

Cooling Zone (E) —The cooling rate should be fast, to keep the solder grains small which will give a longer lasting joint. **Typical cooling rate should be 4 °C.**

17. Ordering Information

17.1 Product Packaging Information

TBD

Figure 13: Product Packaging Information (Plastic Tray)

TBD

Figure 14: Product Packaging Information (Tape)

17.2 Ordering information

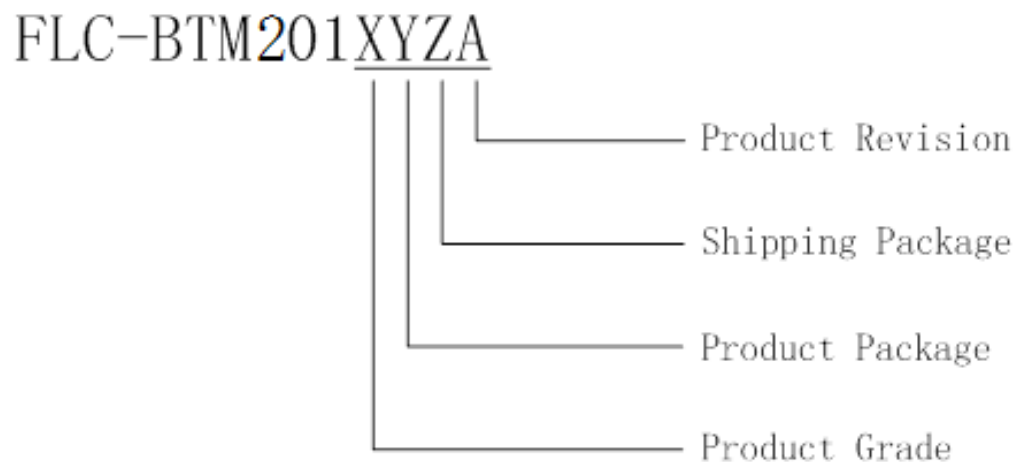


Figure 15: Ordering Information

17.2.1 Product Revision

Product Revision	Description	Availability
A	CSR1024 with antenna	Yes

Table 18: Product Revision

17.2.2 Shipping Package

Shipping Package	Description	Quantity	Availability
0	Foam Tray	—	No
1	Plastic Tray	TBD	Yes
2	Tape	TBD	Yes

Table 19: Shipping Package

17.2.3 Product Package

Product Package	Description	Availability
Q	QFN	No
L	LGA	Yes
B	BGA	No
C	Connector	No

Table 20: Product Package

17.2.4 Product Grade

Product Grade	Description	Availability
C	Consumer	No
I	Industrial	Yes
V	Automobile After-Market	No
A	Automobile Before-Market	No

Table 21: Product Grade