

BLE024V1

Bluetooth Low Energy Module (Based on CSR1024 A06 chip) User Manual and Datasheet

V1.2 2017-11-16

Device Description

- Device Name: BLE024V1
- Bluetooth® low energy technology single mode
 SoC with G.722 Audio Codec, Support BT 5.0
- 16bit RISC MCU, 256 KB internal SPI flash, 80 KB RAM, 192 KB ROM, 60 KB OTP
- 15 digital PIOs, 1 analogue AIO, SPI, I²C, I²S, quadrature decoders, 3D shutter/LED PWM modules, key scanner, LCD glass drive, IR encoder, 10bit Aux ADC
- Support 5 x PWMs LED control
- Ultra low power Bluetooth Low Energy technology radio, V5.0 specification compliant radio
- 23 leads 15.04 x 11.93 x 2 mm, 1.15mm interval stamp bonding pads

Applications

- Bluetooth low energy technology: BT 5.0 support
- HID: keyboards, mice, touchpads, advanced remote controls with voice activation
- Sports and fitness sensors: heart rate, runner/cycle speed and cadence
- Health sensors: blood pressure, thermometer and glucose meters
- Mobile accessories: watches, proximity tags, alert tags and camera controls
- Smart home: heating/lighting control
- Mesh Applications: Support SIG Standard Mesh 1.0

Ordering Information:

Device Name: BLE024V1

Ordering Number: BLE024V1 (with Firmware Version)

Package Type: 1.15mm interval stamp bonding pads +

1.27mm interval DIP Pin Header

Package Size: 23 leads 15.04 x 11.93 x 2 mm

Shipment Pack Method: Plastic Tray
Standard Pack Quantity: to be advice later





INDEX

Ordering Information:	1
1 General Description:	3
2 Device Details:	4
3 BLE024V1 module Functional Block Diagram	5
4 BLE024V1 Module Size and Pins Definitions	5
4.1 Module Size	5
4.2 Module Pins Definitions	6
5 Operating Mods-Power Dissipation Relates	8
5.1 Active	8
5.2 Radio-On	8
5.3 Deep Sleep 30: 16 KB Data RAM and 64 KB RAM Retention	8
5.4 Deep Sleep 20: 16 KB Data RAM Retention	8
5.5 Deep Sleep 10: No RAM Retention and External Interrupts and Timer Enabled	9
5.6 Deep Sleep 00: No RAM Retention and External Interrupts Enabled	9
6 I ² C Master / Slave (General)	9
7 SPI Master / Slave (General)	10
8 SPI Debug Interface	10
9 UART (General)	10
9.1 UART Configuration Settings	11
9.2 UART Configuration while in Deep Sleep	11
10 PWMs	11
10.1 3D Shutter Control PWM	12
10.2 LED Control PWM	12
11 LCD Glass Driver	12
12 Key Scanner	13
13 Quadrature Decoders	13
14 Infrared Output	13
15 Audio	14
15.1 Digital Microphone	14
15.2 G.722 Codec	14
16 10-Bits Aux ADC	14
17 Auxiliary Features	15
17.1 Battery Monitor	15
17.2 Temperature Sensor	15
18 Programable I/Os, PIO and AIO	15
18.1 PIO	15
18.2 AIO	15
18.3 PIO on initial Power Up	16
18.4 LCD Glass Mid-Rail Driver	16
18.5 Analogue Properties of the PIO	16
19 Power Control and Regulation	16



19.1 Switch-mod Regula	ator	16
19.2 Reset		16
20 BLE024V1 module 8	Example Application Schematic	17
21 Electrical Characters		19
21.1 Absolute Maximum	Ratings	19
21.2 Recommend Opera	ating Conditions	20
21.3 Input/Output Term	inal Characteristics	20
21.3.1 Switch-mode	e Regulator	20
21.3.2 RF Liner Reg	ulator	20
21.3.3 Digital I/O Te	erminals	20
21.3.4 AIO		21
22 Current Consumption	on	22
22.1 Theoretical peak po	ower consumption	22
23 Terms and Definition	ns	22
24 Document History		24

1 General Description:

BLE024V1 is a Bluetooth Low Energy technology single mode platform module with ultra-low power consumption. it is based on Qualcomm CSR1024 A06 chip.

Qualcomm® uEnergy™ technology enables ultra-low power connectivity and basic data transfer for applications previously limited by the power consumption, size constraints and complexity of other wireless standards. The uEnergy platform provides everything required to create a Bluetooth low energy technology product with RF, baseband, MCU, qualified Bluetooth v5.0 specification stack and customer applications, for health and fitness sensors, watches, keyboards, mice and advanced remote controls.

BLE024V1 module enables connectivity and data transfer to leading smartphone, tablet and personal computing devices including iOS, Android, Windows, Windows Phone and Blackberry OS devices.

BLE024V1 module supports Qualcomm® Mesh (CSR Mesh). It places the smartphone at the center of the Internet of Things allowing an almost unlimited number of Bluetooth low energy technology enabled devices to be simply networked together and controlled directly from a single smartphone, tablet or PC.

Based on Qualcomm Mesh, BLE024V1 module also support SIG Standard Mesh 1.0

BLE024V1 module meet the requirements of Directive 2011/65/EU of the European Parliament and of the Council on the Restriction of Hazardous Substance (RoHS).



2 Device Details:

Ultra-Low Power Bluetooth Low Energy Technology Radio

- Single pin RF connection (50 impedance in TX and RX modes)
- Requires no external RF components (Certain antennas with gain may require a simple filter)
- Bluetooth v5.0 specification compliant

Bluetooth Transmitter

- 4 dBm RF transmit power
- TX power control
- No external power amplifier or TX / RX switch required

Bluetooth Receiver

- -90.5 dBm sensitivity
- -92 dBm RX Boost mode available: Enhances RX sensitivity at higher receive current cost
- Integrated channel filters
- Digital demodulator for improved sensitivity and co-channel rejection
- Fast AGC for enhanced dynamic range

Bluetooth Stack

- Support for Bluetooth v4.2 specification features:
 - Master and Slave operation
 - Including encryption
- Software stack in firmware includes:
 - GAP
 - L2CAP
 - Security manager
 - Generic attribute protocol
 - Attribute profile
 - Bluetooth low energy technology profile support

Baseband and Software

 Integrated MAC for all packet types enables packet handling without the need to involve the MCU

Audio

- Digital microphone input
- I²S port for PCM I/O
- G.722 Codec

Physical Interfaces

- 11 digital flexible PIOs (including UART RX&TX)
- 4 digital multi-function PIOs with SPI reuse
- 1 analogue AIO (as 3 PIOs with voltage divider)
- UART RX&TX (2 digital flexible PIOs)
- SPI master interface (4 digital multi-function)
- I²C master controller (digital flexible PIOs)
- 4 x quadrature decoders
- PWM 3D shutter control
- 5 x LED PWMs
- Keyboard scanner
- LCD glass drive
- 10-bit Aux ADC
- IR encoder

Auxiliary Features

- Battery monitor
- 6 power modes
- Power management features include software shutdown and hardware wake-up
- Wake-up power management from any PIO
- Integrated switch-mode power supply
- Linear regulator (internal use only)
- AES-128
- Watchdog timer

Memory

- 256 KB internal flash
- 64 KB (Code) and 16 KB (Data) RAM
- 192 KB ROM
- 60 KB OTP
- 256 Byte MTP

Working Voltage

Battery input voltage 3.6 V to 1.4 V

Temperature Specification

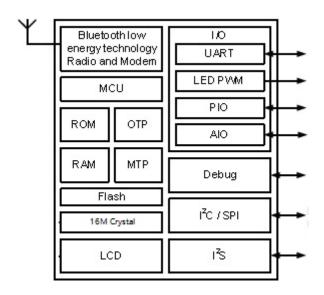
- Standard Operating temperature: -30 to 85 °C
- Extend Operating temperature: -30 to 105 °C
- Storage temperature: -40 to 150 °C

Package

- 23 leads, 15.04 x 11.93 x 2 mm, interval stamp bonding pads +
- Single side routing pinout optimized

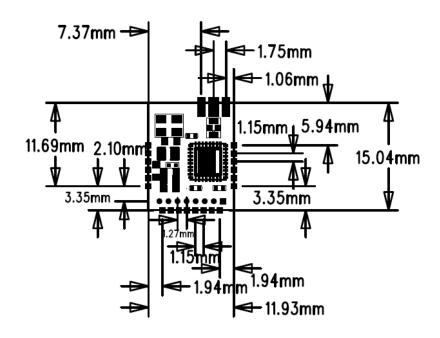


3 BLE024V1 module Functional Block Diagram



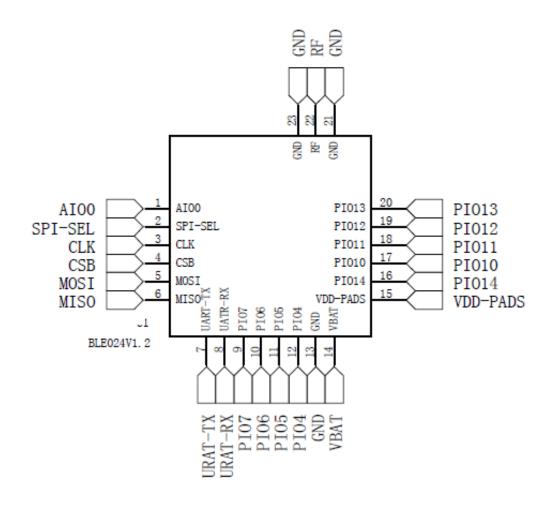
4 BLE024V1 Module Size and Pins Definitions

4.1 Module Size





4.2 Module Pins Definitions



Pin#	Pad	Pad Type	Definitions	Remark
1	AIO0	Unidirectional analogue	Analogue	
			programmable input	
			line	
2	SPI-SEL	Input with strong internal pull-down	Selects Debug SPI	
3	CLK	Debug_SPI_PIO		
4	CSB	Debug_SPI_PIO		
5	MOSI	Debug_SPI_PIO		
6	MISO	Debug_SPI_PIO		
7	UART-TX	Transmit UART data to another device		
8	UART-RX	Receive UART data from another device		
9	PIO7	Digital: Bidirectional with	General programmable	Supply Domain: VDD_PADS
		programmable strength internal pull-	I/O line 7	
		up / pull-down and LCD glass driving		
		capability		
10	PIO6	Digital: Bidirectional with	General programmable	Supply Domain: VDD_PADS
		programmable strength internal pull-	I/O line 6	





		up / pull-down and LCD glass driving capability		
11	PIO5	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 5	Supply Domain: VDD_PADS
12	PIO4	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 4	Supply Domain: VDD_PADS
13	GND	VSS	Ground connections	
14	VBAT	VCC	Positive supply from the battery	
15	VDD-PADS	VDD	Positive supply for PIO and SPI_PIO	
16	PIO14	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 14	Supply Domain: VDD_PADS
17	PIO10	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 10	Supply Domain: VDD_PADS
18	PIO11	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 11	Supply Domain: VDD_PADS
19	PIO12	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 12	Supply Domain: VDD_PADS
20	PIO13	Digital: Bidirectional with programmable strength internal pull-up / pull-down and LCD glass driving capability	General programmable I/O line 13	Supply Domain: VDD_PADS
21	GND	VSS	Ground connections.	
22	RF	Antenna port for Bluetooth transmitter / receiver		
23	GND	VSS	Ground connections.	



5 Operating Mods-Power Dissipation Relates

BLE024V1 module has 6 operating modes. 4 are Deep Sleep modes

Active

Radio-On

Deep Sleep 30: 16 KB Data RAM and 64 KB RAM Retention

Deep Sleep 20: 16 KB Data RAM Retention

Deep Sleep 10: No RAM Retention and External Interrupts and Timer Enabled

Deep Sleep 00: No RAM Retention and External Interrupts Enabled

5.1 Active

In Active mode, the processor runs:

- Code and/or performs activities with peripherals.
- With at least 1 link controller powered.

5.2 Radio-On

In Radio-On mode, the Bluetooth radio is turned on.

NOTE: Radio-On mode can only be entered from Active mode.

5.3 Deep Sleep 30: 16 KB Data RAM and 64 KB RAM Retention

In Deep Sleep: 16 KB Data RAM and 64 KB RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- BLE024V1 supports activity in peripherals to perform a particular operation (e.g. PWMs, keyboard scanner) or wake the chip on activity (e.g. UART, application SPI).
- Link controller state is maintained: this can be active (advertising, scanning or in a connection) and BLE024V1
 can deep sleep between periods on or around radio activity.
- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power controlled using power gating.

5.4 Deep Sleep 20: 16 KB Data RAM Retention

In Deep Sleep: 16 KB Data RAM Retention mode:

- Normal operation uses only the slow clock or intermediate clock (running at a slow speed).
- BLE024V1 supports activity in peripherals to perform a particular operation (e.g. PWMs, keyboard scanner) or wake the chip on activity (e.g. UART, application SPI).
- Link controller state is maintained: this can be active (advertising, scanning or in a connection) and BLE024V1
 can deep sleep between periods on or around radio activity.



- A PIO deep sleep timer time-out or optional temperature change or low battery can wake the chip by generating an interrupt.
- It is possible to keep the processor powered and its power controlled using power gating.

5.5 Deep Sleep 10: No RAM Retention and External Interrupts and Timer Fnabled

In Deep Sleep: No RAM Retention and External Interrupts and Timer Enabled mode:

- VDD_BAT must always be present.
- A PIO can wake the chip (programmable as in Deep Sleep: No RAM Retention and External Interrupts Enabled mode).
- The following can wake BLE024V1 module:
 - PIO hibernate timer time-out.
 - Temperature change.
 - Low battery.

5.6 Deep Sleep 00: No RAM Retention and External Interrupts Enabled

In Deep Sleep: No RAM Retention and External Interrupts Enabled mode:

- An attached battery can be used as a wakeup.
- No timers run, therefore BLE024V1 module can only be woken by a PIO or a rise on VDD_BAT.
- VDD_BAT can be removed if VDD_PADS remain powered, because the pull states of pads are preserved.
- Ignore a rise on VDD_BAT until a PIO has latched an event (enabling 2 different Deep Sleep: No RAM Retention and External Interrupts Enabled modes).
- The PIOs that BLE024V1 module is sensitive to on wakeup are programmable, i.e. it is possible to ignore events on some PIOs but not others

6 I²C Master / Slave (General)

BLE024V1 has 1 I²C master/slave general interface for communication with external peripherals and sensors:

- Maximum clock speed 1 MHz
- Data transmitting/receiving of variable byte length 7-bit and 10-bit addressing modes
- Configurable:
 - PIO pins for SCL and SDA
 - I²C clock: 100 kHz default (software-configurable) at 1:1 duty-cycle (asymmetric if required)
 - Supports slave clock stretching
 - BLE024V1 is Fast Mode and Fast Mode+ compatible.

NOTE: Strong pull is sufficient for I²C on all PIO pads.

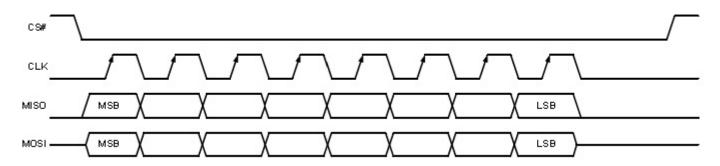


7 SPI Master / Slave (General)

BLE024V1 has 1 SPI master/slave general interface for communication with other devices. It supports:

- SPI master and slave
- All 4 modes supported
- 2 methods of transferring data to memory:
 - DMA to/from memory:
 - ♦ 8-bit or 16-bit word size
 - ◆ Big and little-endian
 - Software reads and writes to FIFOs: variable from 1 to 16 bits
- Interrupt callbacks to processor allow SPI as a slave to indicate that it requires service
- Deep sleep mode (depending on clock)

SPI Timing Diagram



8 SPI Debug Interface

BLE024V1 module uses a 16-bit data and 16-bit address programming and debug interface. Transactions occur when the internal processor is running or is stopped.

SPI Debug Interface is only for the firmware developers use.

9 UART (General)

BLE024V1 module's UART interface provides a simple mechanism to communicate with other serial devices using the RS232 protocol.

UART Signals

Signal	Description
UART_RX	Pin to receive UART data from another device



UART_TX	Pin to transmit UART data to another device
UART_CTS	Pin to notify another device BLE024V1 is ready to receive data (active low input)
UART_RTS	Pin to notify other device BLE024V1 is ready to send data (active low output)

9.1 UART Configuration Settings

UART configuration parameters, e.g. baud rate and data format, are set using BLE024V1 firmware.

NOTE To communicate with the UART at its maximum data rate using a standard PC, the PC requires an accelerated serial port adapter card.

UART Configuration Settings

Parameter Possible Values	
Baud rate Minimum	1200 baud (≤2 % Error)
Baud rate Minimum	9600 baud (≤1 % Error)
Baud rate Maximum (XTAL)	1M baud (≤1 % Error)
Parity	None, Odd or Even
Number of stop bits	1 or 2
Bits per byte	8

9.2 UART Configuration while in Deep Sleep

The maximum baud rate is 2400 baud during deep sleep.

10 PWMs

BLE024V1 has 5 independently configurable PWM instances.

A multipurpose PWM generator provides 3 modes:

- Normal PWM mode:
 - For motor control and general purpose PWM
- 3D Shutter mode:
 - For 3D shutter control
 - Cycle accurate
 - 16-bit resolution for all the configuration registers to be specified in clock cycles
 - New configuration applied on update register write or at a specific time (e.g. in response to radio traffic)
 - Variable offset after the reconfiguration can be applied
 - Configurable width of the external sync pulses
- LFD mode
 - For LED fading



10.1 3D Shutter Control PWM

To be advice later

10.2 LED Control PWM

BLE024V1 has 4 LED mode PWM blocks (2 x fast / 2 x slow). Each LED mode PWM has an 8-bit resolution for all configuration registers and a:

- Minimum brightness duty cycle (grouped in a 16-bit wide register)
- Maximum brightness duty cycle (grouped in a 6-bit wide register)
- Hold Minimum and Maximum time (grouped in a 16-bit wide register)
- Step (ramp) time
- Brightness configuration specified in units of typically 30 μs assuming a 32 kHz clock
- Hold times specified in units of typically 16 ms assuming a 32 kHz clock
- Step time specified in units of typically 1 ms assuming a 32 kHz clock

NOTE: BLE24 supports immediate reconfiguration on the sync register write.

11 LCD Glass Driver

BLE024V1's LCD driver has the following features:

- Drives simple static and multiplexed LCD glass with no requirement for external components.
- Capable of controlling PIO pads to support bias modes:
 - Normal: Switching between GND and VCC
 - 1/2 bias: Switching between GND, 1/2 VCC and VCC
 - 1/3 bias: Switching between GND, 1/3 VCC, 2/3 VCC and VCC
- Up to 28 segments and 4 common (backplane) driver outputs
- Configurable to support non-multiplexed (static) and 2, 3 or 4 way multiplexed LCD glass
- Supports LCD glass with up to 112 display segments (4x the number of segment driver outputs)

NOTE: Unused segment outputs that can be disabled.

- LCD blanking support: Enables flashing of all segments at slow (typically 2 Hz) frequency
- LCD segment blinking support: Up to 2 segments can be configured to blink at slow frequency (typically 2 Hz)
- Flexible input clock pre\(\text{D}\)scaler to support required clock frequencies for different multiplexing modes and LCD glass characteristics.
- Ultra-low power operation to maintain LCD display with only low frequency clock input (typically 32 kHz)
- LCD clock output for pad drivers to increase output pad drivers when LCD output changes.
- Contrast control



12 Key Scanner

BLE024V1 has 1 key scanner for applications such as mouse and keyboard HID.

Physical buttons are located on line crossings A to F. If a button is pressed both lines become connected. Assuming sense lines are pulled-up by internal logic, a key press, for example C can be detected by forcing PIO[OUT1] loward reading 0 on PIO [IN 0].

It supports:

- Keypad matrix up to 12 PIO inputs (sense lines) and 18 PIO outputs (drive lines):
 - Drives 1 to 18 drive lines consecutively12□bit key registers updated every scan
 - Press and release events reported to the host via callback
- Variable scan rate:
 - By default, drives consecutive drive lines every clock cycle
 - Configurable number of clocks per drive line

NOTE: The key scanner does not support ghost key removal.

The key scanner configuration and control includes:

- PIO pin numbers to be used for drive and sense lines
- Scan rate, Hz and active/idle ratioHardware starting and stopping
- Callback creation to receive keyboard map data.

13 Quadrature Decoders

BLE024V1 module has 4 quadrature decoders with:

- Each having a configurable simple filter on inputs (for debouncing)
- Enabling and disabling of single or multiple decoders
- Data reading functionality
- Processor interrupt generation

14 Infrared Output

BLE024V1 module has 1 IR output for applications such as infrared remote control. It can run from Fast XTAL and Intermediate clocks.



15 Audio

NOTE: Digital microphone and I²S input cannot be active at the same time. G.722 codec cannot encode and decode at the same time.

15.1 Digital Microphone

BLE024V1 module has 1 digital microphone input with:

- 1 or 2 Mbps sample rate
- Software selectable as left or right channel
- G.722 encoder or bypass option
- Audio routed to firmware only (not to I²S)
- Software supporting DMIC clock frequencies of 500 kHz, 1 MHz, 2 MHz, and 4 MHz

15.2 G.722 Codec

BLE024V1 module has a G.722 Codec, featuring:

- Output: 48 kbps (optional 56 or 64 kbps)
- Input: 16 kHz/16□bits (optional 8 kHz/8-bits, 8 kHz/16-bits and 16 kHz/8-bits)
- Output produces 20 Byte blocks for easy GATT streaming

NOTE: Analogue audio is not provided.

16 10-Bits Aux ADC

BLE024V1 module has 1 10-bit Aux ADC:

- A resistive SAR ADC
- Attached to 1 AIO pad
- The processor has access to its ADC result value after exit from Deep Sleep mode

NOTE: The 10-bit Aux ADC is not available during XTAL startup or battery voltage and temperature monitoring. Therefore, the time to perform a conversion may be longer if the hardware is already using the ADC.



17 Auxiliary Features

17.1 Battery Monitor

BLE024V1 module contains an internal battery monitor that reports the battery voltage to the software.

17.2 Temperature Sensor

CSR1024 LGA contains a temperature sensor that measures the temperature of the die and can report the chip temperature in °C or Kelvin using a firmware API.

BLE024V1 module could report the temperature of CSR1024 chip through the UART or BLE interface.

NOTE: This feature may not be available in the current firmware.

18 Programable I/Os, PIO and AIO

18.1 PIO

15 lines of programmable bidirectional I/O are provided:

- May be set by the application code or used as an input or to wake the chip.
- Software-configurable as weak pull-up, weak pull-down, strong pull-up or strong pull-down.
- At reset all lines are inputs with weak pull-down.
- Pull strength, direction and pad states preserved across all non-off states to support waking on any PIO
 (even when VDD_DIG is powered down). Configurable to wake CSR1024 LGA via an individually selectable
 mask for rising, falling or any edge transition from Deep Sleep modes.
- Available as interrupt request lines.
- Powered from VDD PADS

NOTE: VDD PADS must remain powered.

QTIL cannot guarantee that the PIO assignments remain as described. Implementation of the PIO lines is firmware build-specific, for more information see the relevant software release note.

18.2 AIO

BLE024V1 module has 1 pin providing a unidirectional analogue programmable input line, AIO[0]. NOTE: This pin does not provide an output capability.



18.3 PIO on initial Power Up

Pull-Up and Pull-Down default to weak values unless specified otherwise.

Pin Name / Group	On Initial Power Up		
SPI_PIO#	Strong Pull-Down		
All other PIOs	Weak Pull-Down		

18.4 LCD Glass Mid-Rail Driver

BLE024V1 supports direct LCD glass driving by internally generating required voltage for one of the following modes of operation:

1/2 mode

1/3 and 2/3 mode

Voltage levels are generated and routed internally to the I/O pads configured for LCD glass driving. NOTE: Only a single mode of operation is available.

18.5 Analogue Properties of the PIO

Most BLE024V1 module PIOs can route in an analogue signal that can be digitised using the 10-bit Aux ADC. NOTE: This feature may not be available in the current firmware.

19 Power Control and Regulation

BLE024V1 module contains a switch-mode regulator that generates all the supply rails required from the battery.

19.1 Switch-mod Regulator

The switch-mode regulator generates the main rail from the battery supply, VDD BAT.

The switch-mode regulator generates all required voltage rails for the system to operate using only a single inductor.

No user intervention is required because the regulator automatically changes from buck to boost mode depending on the battery voltage and output voltage of the rail(s).

19.2 Reset

BLE024V1 module is reset by:

- Power-on reset
- Software-configured watchdog timer
- Command through UART interface from other MCU or control devices

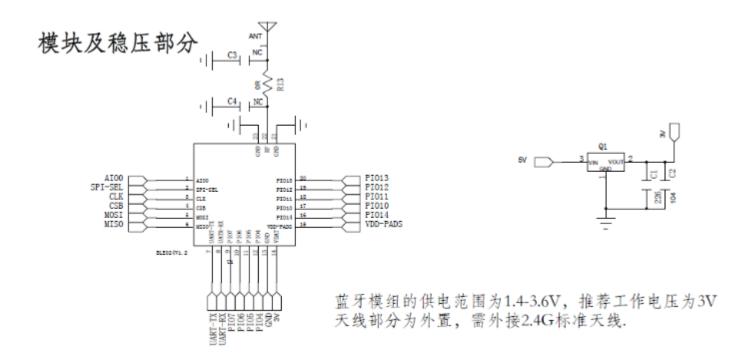


• Command through BLE interface from Smartphone devices or other BLE devices NOTE:

VDD_BAT input voltage must drop to 0.4 V to guarantee a rising VDD_BAT is seen by the PMU on reassertion. VDD_BAT takes approximately 20 s to drop to 0 V when power is removed due to circuit decoupling capacitance. To fully reset the PIO pads take all VDD_PADS pins below 0.4 V.

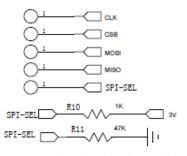
20 BLE024V1 module Example Application

Schematic



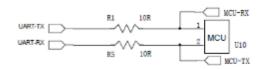


SPI 引脚部分



当SPI-SEL这个引脚下拉时,这4个SPI 引脚是可以当普通PIO来用 当SPI-SEL这个引脚外部上拉时此时这 4个引脚只能当作烧录跟调试端口

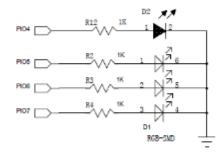
串口通信部分



模组串口的工作电压为3V,当 与不同电平规格的串口通信时 需要进行电平转换

注: 串口也可当作普通PIO来用

PIO输出部分



PIO输出PWM信号用做LED RGBW和蜂鸣器 的控制,也可输出高低电平用做其它的控制



按键复位部分



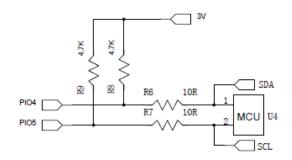
按键可用来做开关机, 复位,唤醒等功能

AIO模拟采集部分



AIO采集的模拟量数据是电压 采集的最高电压为1.26V

PIO模拟I2C通信部分



21 Electrical Characters

21.1 Absolute Maximum Ratings

Rating	Min	Тур	Max	Unit
Storage temperature	-40		85	°C
Battery (VDD_BAT and VDD_PADS)	0		3.6	V
I/O supply voltage	0		3.6	V
I/O supply (VDD_PADS) total current			30	mA



	1	1		
VDD_AUX, VDD_DIG, AIOs	0		1.26	V

21.2 Recommend Operating Conditions

Operating condition	Min	Тур	Max	Unit
Operating temperature range	-30	20	85	°C
Battery (VDD_BAT)	1.4	3	3.6	V
I/O supply voltage (VDD_PADS)	1.4	3	3.6	V

21.3 Input/Output Terminal Characteristics

Always comply with the stated values when attaching external components to BLE024V1. NOTE Current drawn by a pin is positive (+ve), current supplied is negative (-ve).

21.3.1 Switch-mode Regulator

Switch-mode Regulator	Min	Тур	Max	Unit
Output voltage (VDD_AUX)(1)	-	1.2	-	V
Output voltage (VDD_DIG)(1)	-	1.1	-	V
Output voltage (VDD_RAD)(1)	-	1.8	-	٧
Output voltage (VDD_MEM)(1)	-	3.3	-	V

NOTE 1. These are internal regulators and should have no additional load connected.

21.3.2 RF Liner Regulator

Normal Operation	Min	Тур	Max	Unit
Input voltage (VDD_RF_IN)	1.2	-	2.2	٧
Output voltage (VDD_RF)	1.0	1	2.0	٧

NOTE This regulator is for QTIL internal use only of the RF rail.

21.3.3 Digital I/O Terminals

Input Voltage Levels

Input Voltage Levels	Min	Тур	Max	Unit
VIL input logic level low	-	ı	25% x VDD_PADS	V
VIH input logic level high	75% x VDD_PADS	-	-	V

Output Voltage Levels

Output Voltage Levels	Min	Тур	Max	Unit
-----------------------	-----	-----	-----	------



VOL output logic level low, IOL = 8.0 mA (Max Drive Strength)	-	-	20% x VDD_PADS	V
VOH output logic level high, IOL = -8.0 mA (Max Drive Strength)	80% x VDD_PADS	-	-	V
Tr/Tf (for 30 pF load)	-	-	2	ns

Input and Tristate

Input and Tristate	Min	Тур	Max	Unit
With strong pull-up	3.5	4.7	6.0	kΩ
With strong pull-down	3.5	4.7	6.0	kΩ
With weak pull-up(1)	8	40	50	μΑ
With weak pull-down(1)	10	40	50	μΑ
CI input capacitance	-	5	-	pF

NOTE 1. Range applicable for VDD_PADS between 1.8 V and 3.3 V when measured as a short circuit.

21.3.4 AIO

Input/Output Voltage Levels	Min	Тур	Max	Unit
Input voltage	0	-	VDD_AUX	V

21.3.4.1 10-Bits AUX ADC

10-bit Aux ADC	Min	Тур	Max	Unit
Resolution	-	-	10	Bits
Input voltage range(1)	0	-	VDD_AUX	V
Input bandwidth	-	100	-	kHz
Conversion time	1.38	1.69	4.14	μs
Sample rate(2)	-	-	700	Samples/s

NOTE

- 1. LSB size = $VDD_AUX/1023$.
- 2. The 10-bit Aux ADC is accessed through the firmware API. The sample rate given is achieved as part of this function.

21.4 ESD Protection

Apply ESD static handling precautions during manufacturing.

Condition	Class	Max Rating
Human Body Model Contact Discharge per JEDEC EIA /JS-001-2014	1C	2 kV (all pins except RF rated at 1 kV) (1)
Charged Device Model Contact Discharge per JEDEC EIA /JS002-2014	C1	500 V (all pins) (1)

NOTE 1. This value is preliminary and may be subject to change.



22 Current Consumption

22.1 Theoretical peak power consumption

Mode	Description	Total Typical
		Current at 3 V
Deep Sleep: No RAM Retention	All functions are shut down.	1.6-2 μΑ
and External Interrupts Enabled	To wake the chip, toggle a pre-configured PIO.	
Deep Sleep: No RAM Retention	VDD_PADS = ON	5.5 μΑ
with External Interrupts and Timer	VDD_BAT = ON	
Enabled		
Deep Sleep: 16 KB Data RAM	VDD_PADS = ON	10.5 μΑ
Retention	VDD_BAT = ON	
	RAM = ON	
	Digital Circuits = ON	
	SMPS = ON	
Deep Sleep: 16 KB Data RAM and	VDD_PADS = ON	12 μΑ
64 KB RAM Retention	VDD_BAT = ON	
	RAM = ON	
	Digital Circuits = ON	
	SMPS = ON	
Idle: Shallow Sleep	VDD_PADS = ON	0.75 mA
	VDD_BAT = ON	
	RAM = ON	
	Digital Circuits = ON	
	MCU = IDLE	
	<1µs Wake-up Time	
Idle: Active	VDD_PADS = ON	1.3 mA (Execution
	VDD_BAT = ON	from Cache)
	RAM = ON	
	Digital Circuits = ON	13.5 mA (Active
	MCU = IDLE	SMEM Execution)
	<1μs Wake-up Time	
TX Active	4 dBm Transmit Power	5 mA Average
RX Active	-90.5 dBm Sensitivity	5 mA Average

23 Terms and Definitions

Term Definition





ADC	Analogue to Digital Converter
AES	Advanced Encryption Standard
AGC	Automatic Gain Control
AIO	Analogue Input/Output
ATT	ATTribute protocol
В	Byte
Bluetooth®	Set of technologies providing audio and data transfer over short \exists range radio
	connections
Qualcomm® BlueCore™	Group term for QTIL's range of Bluetooth wireless technology ICs
codec	Coder decoder
CSR™	Cambridge Silicon Radio
dBm	Decibels relative to 1mW
EIA	Electronic Industries Alliance
ESD	Electrostatic Discharge
GAP	Generic Access Profile
GATT	Generic ATTribute protocol
GSM	Global System for Mobile communications
HID	Human Interface Device
I ² C	Inter-Integrated Circuit Interface
I ² S	Inter-Integrated Circuit Sound
1/0	Input/Output
IC	Integrated Circuit
IF	Intermediate Frequency
IPC	See www.ipc.org
JEDEC	Joint Electron Device Engineering Council (now the JEDEC Solid State Technology
	Association)
KB	Kilobyte
L2CAP	Logical Link Control and Adaptation Protocol
LCD	Liquid-Crystal Display
LDO	Low (voltage) Drop-Out
LED	Light-Emitting Diode
LGA	Land Grid Array
LNA	Low Noise Amplifier
MAC	Medium Access Control
MCU	MicroController Unit
MISO	Master In Slave Out
MOSI	Master Out Slave In
MTP	Multiple-Time Programmable
NC	Not Connected or No Connection
NSMD	Non-Solder Mask Defined
NVM	Non-Volatile Memory
ОТР	One-Time Programmable
PA	Power Amplifier
PC	Personal Computer



PCB	Printed Circuit Board
PCM	Pulse Code Modulation
PIO	Programmable Input/Output, also known as general purpose I/O
PMU	Power Management Unit
ppm	parts per million
PWM	Pulse Width Modulation
QTIL	Qualcomm Technologies International, Ltd.
RAM	Random Access Memory
RF	Radio Frequency
RISC	Reduced Instruction Set Computer
RoHS	Restriction of Hazardous Substances in Electrical and Electronic Equipment Directive
	(2002/95/EC)
ROM	Read Only Memory
RSSI	Received Signal Strength Indication
RX	Receive or Receiver
SDK	Software Development Kit
SMPS	Switch-Mode Power Supply
SPI	Serial Peripheral Interface
TX	Transmit or Transmitter
UART	Universal Asynchronous Receiver Transmitter
VCO	Voltage Controlled Oscillator
W-CDMA	Wideband Code Division Multiple Access

24 Document History

Revision	Date	Change Reasons
1.0	2017-01-06	Original First Release
1.1	2017-04-11	Add 1.27mm interval DIP Pin Header
1.2	2017-09-14	Update ANT pin contactors
		Change a GND pin to a general PIO
		Update CSR1024 from A05 to A06
		Support BT 5.0
		Update Example Application
		Schematic in Chinese
		Update Power Consumptions
	2017-11-16	SPI-SEL pull-up resistor change to 1k
		ohm