



Qualcomm Technologies, Inc.

WCD9335 Audio Codec

Device Specification

LM80-P2751-29 Rev. A

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Revision history

Revision	Date	Description
A	February 2018	Initial release

1 Introduction

1.1 Device description

This document contains a description of the chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE Enabling some features may require additional licensing fees.

The WCD9335 is a stand-alone high fidelity (hi-fi) audio codec IC that supports the Qualcomm Technologies, Inc. (QTI) multimedia solutions, including the APQ8096SGE chipset. The key WCD9335 functions include the following:

- Serial low-power interchip media bus (SLIMbus) for access to all on-chip digital audio channels; inter-IC sound (I²S) accesses fewer paths, but maintains compatibility with earlier integrated circuits (ICs).
- SoundWire interface for driving WSA8810 or WSA8815 speaker amplifiers
- Six analog input ports and seven analog output ports
- Six audio analog-to-digital converters (ADCs) and seven digital-to-analog converters (DACs)
- Six digital microphone inputs (three clock/data pairs)
- Multibutton headset control (MBHC) for smart accessory detection
- Digital processing includes the following:
 - Microphone activity detection (MAD) detecting audio, ultrasound, and beacon activity
 - Qualcomm[®] Voice Activation subsystem
 - Active noise cancellation (ANC)
- Integrated analog support reduces bill of materials (BOM) and area:
 - Microphone bias outputs (x4)

1.2 Summary of key features

WCD9335 features are listed in [Table 1-1](#).

- Lower cost, smaller footprint while enabling high-percentage digital content
- Ultra low-power voice activation engine for keyword detection and user identification
- Low-power, high-performance ultrasound support, including analog microphone (MIC) and line output

- Hi-fi audio recording and playback – 109 dB ADC and 130 dB DAC signal-to-noise ratio (SNR)
- 32-bit/384 kHz, 44.1 kHz processing
- Supports external smart speaker amplifiers such as WSA8810/WSA8815 with 2-wire SoundWire signaling to provide configuration flexibility and reduce printed circuit board (PCB) design complexity.
- Class-H headphone amplifier – 122 dB dynamic range and -105 dB THD+N
- MBHC, including an additional pad to support both tip and ground insertion/removal
- Ground reference pad for line outputs to improve signal integrity for docking stations.
- Only two external supplies are required; all other required voltages are generated by the WCD9335 support circuits.
- Highly integrated 4.17 × 3.91 mm fan out wafer-level picoscale package (FOWPSP)

See [Section 1.5](#) for a complete list of the WCD9335 features.

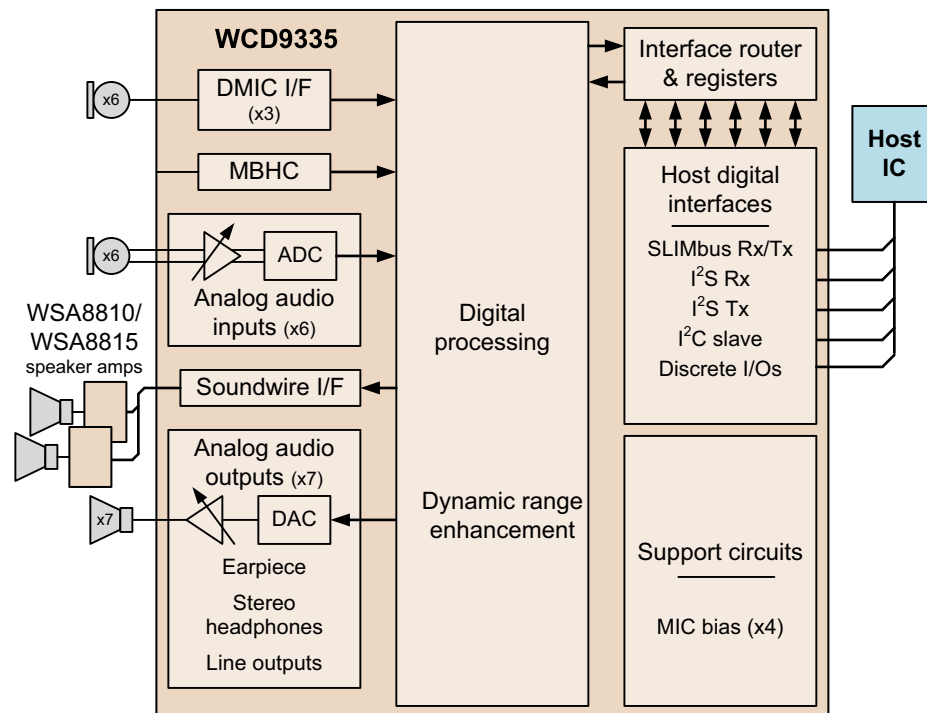


Figure 1-1 WCD9335 high-level block diagram

1.3 WCD9335 detailed functional block diagram

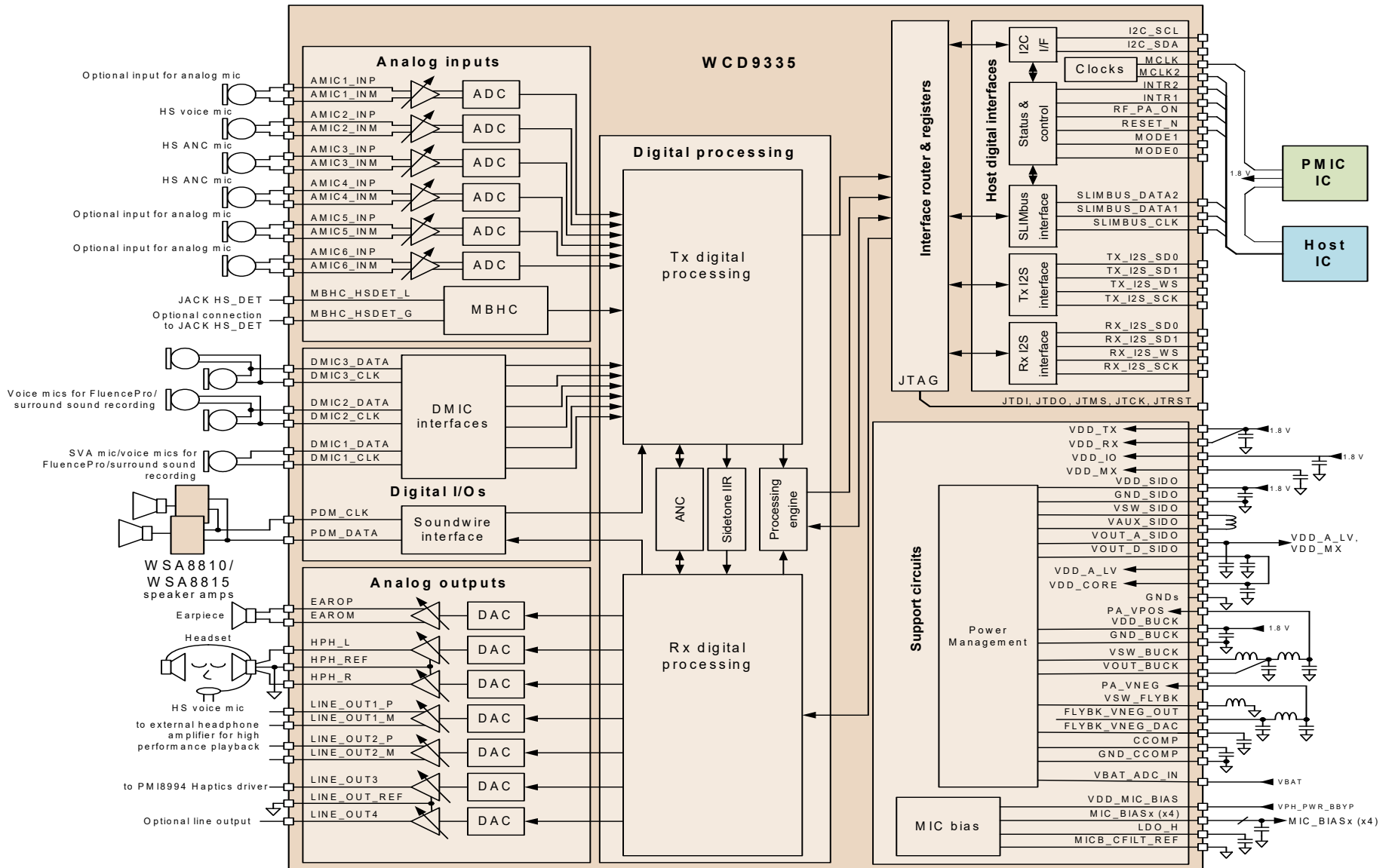


Figure 1-2 WCD9335 detailed functional block diagram

1.4 Supply voltage summary

The following supplies are required:

- Primary phone power (VPH_PWR)
- Regulated 1.8 V from power management

The on-chip circuits generate all other voltages required by the WCD9335.

1.5 Features

The features of the WCD9335 device are listed in [Table 1-1](#).

Table 1-1 Summary of WCD9335 device features

Feature	WCD9335 capabilities
System	
Hi-fi audio	<ul style="list-style-type: none"> ■ Recording path: 110 dB dynamic range and -103 dB THD + N ■ Playback path: 130 dB dynamic range and -109 dB THD + N
Qualcomm Voice Activation subsystem	<ul style="list-style-type: none"> ■ Microphone activity detection (MAD) to detect audio and beacon activity ■ Codec processing engine (CPE) with 304 kB on-chip RAM ■ Provides keyword detection and user identification in the codec with less than 0.85 mA power at battery (100% speech occupancy). ■ Look-ahead buffer provides more consistent and coherent interaction to users.
Digital I/Os	
SLIMbus slave	<ul style="list-style-type: none"> ■ Two data lanes; 16 transmit (Tx) ports + 8 receive (Rx) ports + control ■ Tx sample rates: 8, 16, 32, 48, 96, and 192 kHz ■ Rx sample rates: 8, 16, 32, 44.1, 48, 96, 192, and 384 kHz ■ Bit resolution: 12, 16, 20, 24, and 32 ■ Framer device to support framer handover to codec
Two stereo master and slave I ² S	<ul style="list-style-type: none"> ■ Isochronous mode ■ Push/pull transport protocols ■ Four Tx ports + four Rx ports ■ Tx sample rates: 8, 16, 32, 48, 96, and 192 kHz ■ Rx sample rates: 8, 16, 32, 44.1, 48, 96, and 192 kHz ■ Bit resolution: 16 and 32
SoundWire interface to WSA8810/WSA8815	<ul style="list-style-type: none"> ■ Multichannel, audio, and control use two lines (one clock and one data)
Digital microphone ports	<ul style="list-style-type: none"> ■ Six; three clock lines; nine supported frequencies from 600 kHz to 6.144 MHz
Interrupts	<ul style="list-style-type: none"> ■ Multiple hardware interrupts multiplexed behind two interrupt pads

Feature	WCD9335 capabilities
<i>Tx processing</i>	
Analog audio input ports	<p>Six ports that support differential and single-ended configurations. There are three operational modes:</p> <ul style="list-style-type: none"> ■ Hi-fi <ul style="list-style-type: none"> □ Programmable gain from 0–24 dB in 1.5 dB steps □ 0.9 μVrms input referred noise, 100 dB SNR, and -107 THD at 21 dB gain ■ Standard <ul style="list-style-type: none"> □ Programmable gain from 0–30 dB in 1.5 dB steps □ 1.4 μVrms input referred noise, 96 dB SNR, and -102 THD at 21 dB gain ■ Ultra low power <ul style="list-style-type: none"> □ Programmable gain from 0–30 dB in 1.5 dB steps □ 2.7 μVrms input referred noise, 90 dB SNR, and -95 THD at 21 dB gain <p>Capless inputs:</p> <ul style="list-style-type: none"> ■ Input multiplexing allows routing any AMIC input to any decimator ■ Integrated IEC diodes on AMIC2_INP, AMIC3_INP, and AMIC4_INP
ADCs	<ul style="list-style-type: none"> ■ Six audio ADCs
Concurrency	<ul style="list-style-type: none"> ■ Nine concurrent Tx decimation paths to support voice and audio applications
Digital controls	<ul style="list-style-type: none"> ■ Gain: -84 dB to +40 dB in 0.5 dB increments ■ DC blocking corner frequency: 4 Hz, 75 Hz, and 100 Hz
Decimation filters	<ul style="list-style-type: none"> ■ Nine decimation filters for concurrent Tx paths ■ Passband ripple: \pm 0.005 dB
<i>Rx processing</i>	
Analog audio output ports	<ul style="list-style-type: none"> ■ Seven – earpieces, stereo headphone, four line outputs (two differentials, two single-ended or four single-ended) ■ Integrated IEC diodes on EAROP, EAROM, HPH_L, HPH_R, and HPH_REF pads ■ Class-H differential earpiece output <ul style="list-style-type: none"> □ 120 mW (typical) into 32 Ω; 150 mW (minimum) into 16 Ω or 10.67 Ω ■ Class-H stereo single-ended headphone outputs; capless; 16 Ω or 32 Ω ■ Two differentials and two single-ended line outputs
Digital audio to WSA	<ul style="list-style-type: none"> ■ SoundWire interface
DACs	<ul style="list-style-type: none"> ■ Seven DACs and nine dedicated interpolators ■ High-performance DACs for differential line outputs (to external headphone amplifiers)
Performance	<ul style="list-style-type: none"> ■ Headphone: 1 Vrms; 122 dB dynamic range, -105 dB THD+N, and 16 μVpp click and pop in Class-H mode ■ Line outputs: 2 Vrms; 130 dB dynamic range and -109 THD+N (differential)
Concurrency	<ul style="list-style-type: none"> ■ Nine concurrent Rx paths
Frequency response	<ul style="list-style-type: none"> ■ High pass filter (HPF) cutoff of 0.48 Hz with 0.0025 dB droop at 20 Hz to meet Dolby requirements ■ Nine interpolation filters with passband ripple of \pm0.0025 dB (HPF disabled)
Mixing	<ul style="list-style-type: none"> ■ Digital mixing at the input of each DAC path ■ Digital mixing on inputs to IIRs with independent gain control ■ HD audio mixing path added to all interpolators

Feature	WCD9335 capabilities
Dynamic range enhancement	<ul style="list-style-type: none"> ■ DRE provides Hi-Fi audio quality for headphone and line-output PAs
Protection and suppression	<ul style="list-style-type: none"> ■ Overcurrent protection ■ Click-and-pop suppression
Multiple sample rates	<ul style="list-style-type: none"> ■ Any path can use any of these sampling rates: 8, 16, 32, 44.1, 48, 96, 192, and 384 kHz
Concurrent PCM rates	<ul style="list-style-type: none"> ■ Independent rates on each path to support voice and music concurrently
Additional digital processing and paths	
Active noise cancellation	–
Multibutton headset control (MBHC)	<ul style="list-style-type: none"> ■ Moisture detection ■ Mechanical plug insertion and removal detection on both tip and ground detection pad with pop noise reduction ■ Accessory plug type (3-pole, 4-pole - CTIA or OMTP, and 5-pole) detection ■ Detection for up to eight buttons (send/end, volume, and play control) ■ Headset impedance detection with $\pm 5\%$ from 3 Ω up to 2 kΩ
Sidetone paths and processing	<ul style="list-style-type: none"> ■ All mixed channels operate at the same sample rate ■ No gain changes occur as a result of mixing channels ■ Five-stage IIR filters ■ Sample-rate converters ■ Echo cancellation (EC)
Clock circuits	<ul style="list-style-type: none"> ■ Master clocks supported: 24.576, 19.2, 12.288, and 9.6 MHz (default)
Support circuits	
Microphone biasing	<ul style="list-style-type: none"> ■ Four voltage sources for powering analog and digital microphones ■ Programmable from 1.0 V to 2.85 V
SmartBoost	<ul style="list-style-type: none"> ■ Feedback signal to the companion WSA boost for efficient power control
Feedback speaker protection	<ul style="list-style-type: none"> ■ Receives I/V sense signals from companion WSA devices and transmits them to the audio processing in the APQ chipset
Always-on power	<ul style="list-style-type: none"> ■ Supports headset-insert/button-detect and Snapdragon Voice Activation while in low-power sleep mode
Fabrication technology and package	
Package	<ul style="list-style-type: none"> ■ Small, thermally efficient 113 FOWPSP; 4.17 × 3.91 × 0.65 mm; 0.35 mm pitch

1.6 Terms and acronyms

Table 1-2 defines terms and acronyms commonly used throughout this document.

Table 1-2 Terms and acronyms

Term or acronym	Definition
ADC	Analog-to-digital converter
AMIC	Analog microphone

Term or acronym	Definition
BOM	Bill of materials
BPF	Band pass filter
bps	Bits per second
CPE	Codec processing engine
DAC	Digital-to-analog converter
DMIC	Digital microphone
EC	Echo cancellation
ESD	Electrostatic discharge
FOWPSP	Fan out wafer-level picoscale package
FOWL	Fan out wafer level package
Hi-fi	High fidelity
HPF	High pass filter
HPH	Headphone
HR	Hundred reel
HV	High voltage
I ² C	Interintegrated circuit
I ² S	Inter-IC sound
IEC	International Electrotechnical Commission
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1990)
LDO	Low dropout (linear regulator)
LPF	Low pass filter
LV	Low voltage
MBHC	Multibutton headset control
MGB	Master bandgap (voltage reference)
MIC or mic	Microphone
MSL	Moisture sensitivity level
NVM	Nonvolatile memory
OEM	Original equipment manufacturer
OSR	Oversampling ratio
PA	Power amplifier
PCB	Printed circuit board
PDM	Pulse density modulation
RoHS	Restriction of hazardous substances
SIDO	Single inductor dual output
SIMO	Single inductor multiple outputs
SLIMbus	Serial low-power interchip media bus

Term or acronym	Definition
SMPS	Switched-mode power supply
SMT	Surface-mount technology
SNR	Signal-to-noise ratio
Sn/Ag/Cu	Also known as SAC. Tin-silver-copper is a lead-free (Pb-free) alloy commonly used for electronic solder
SPKR	Speaker
SR	Short reel
TR	Tape and reel
WCD	WSP codec device
WLP	Wafer-level package
WSA	WSP smart amplifier
WSP	Wafer-scale package
XO	Crystal oscillator

2 Pad definitions

The WCD9335 is available in the 113 FOWPSP; a high-level view of its pad assignments is shown in Figure 2-1.

1 DNC		2 GND_ SIDO		3 VBAT_ ADC_IN		4 PDM_ _DATA		5 DMIC2_ _CLK		6 JTDI		7 TX_I2S_ _SD0		8 GND
	9 VSW_ _SIDO		10 MIC_ BIAS3		11 PDM_ _CLK		12 SLIMBUS_ _DATA2		13 VDD_ _MX		14 RX_I2S_ _SCK		15 RX_I2S_ _SD0	
16 VDD_ _SIDO		17 MIC_ BIAS4		18 MIC_ BIAS1		19 TX_I2S_ _SCK		20 DMIC3_ _DATA		21 VDD_ _IO		22 VDD_ _CORE		23 TX_I2S_ _WS
	24 GND_ _SIDO		25 MIC_ BIAS2		26 RESET_N		27 SLIMBUS_ _DATA1		28 GND		29 RX_I2S_ _SD1		30 GND	
31 VAUX_ _SIDO		32 LDO_H		33 MICB_ CFILT_ _REF		34 SLIMBUS_ _CLK		35 VDD_ _CORE		36 DMIC3_ _CLK		37 VDD_ _MX		38 TX_I2S_ _SD1
	39 VOUT_ _A_SIDO		40 VDD_ MIC_BIAS		41 INTR1		42 VDD_ _CORE		43 DMIC1_ _CLK		44 JTMS		45 JTDO	
46 VOUT_ _D_SIDO		47 GND_ _TX		48 CCOMP		49 GND		50 DMIC1_ _DATA		51 JTCK		52 VDD_ _CORE		53 VDD_ _IO
	54 AMIC6_ _INM		55 VDD_ _A_LV		56 INTR2		57 GND		58 DMIC2_ _DATA		59 GND		60 GND	
61 AMIC6_ _INP		62 VDD_ _TX		63 GND_ _CCOMP		64 GND		65 GND		66 I2C_ _SCL		67 I2C_ _SDA		68 RX_I2S_ _WS
	69 AMIC5_ _INP		70 AMIC5_ _INM		71 MCLK		72 MCLK2		73 RF_PA_ _ON		74 JTRST		75 VSW_ _BUCK	
76 AMIC4_ _INP		77 AMIC4_ _INM		78 MBHC_ _HSDDET_G		79 MODE1		80 GND		81 GND		82 VOUT_ _BUCK		83 VDD_ _BUCK
	84 AMIC3_ _INP		85 AMIC3_ _INM		86 LINE_ _OUT2_M		87 MODE0		88 HPH_REF		89 MBHC_ _HSDDET_L		90 GND_ _BUCK	
91 AMIC2_ _INP		92 AMIC2_ _INM		93 LINE_ _OUT_REF		94 LINE_ _OUT1_P		95 GND_ _RX		96 VDD_ _RX		97 PA_ _VPOS		98 VSW_ _FLYBK
	99 AMIC1_ _INM		100 LINE_ _OUT4		101 LINE_ _OUT2_P		102 EAROP		103 HPH_R		104 PA_ _VNEG		105 FLYBK_ _VNEG_ _OUT	
106 GND		107 AMIC1_ _INP		108 LINE_ _OUT3		109 LINE_ _OUT1_P		110 EAROM		111 HPH_L		112 FLYBK_ _VNEG_ _DAC		113 DNC

Analog audio inputs	Analog audio outputs	Digital I/Os	Host digital interfaces	Support circuits	DNC	Power	Ground
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Figure 2-1 WCD9335 pad assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input
AO	Analog output
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
Z	High-impedance (Hi-Z) output
VDD_IO is used for digital I/O pads.	

2.2 Pad descriptions

Descriptions of all pads are presented in the following tables, organized by functional group:

- [Table 2-2](#) Analog inputs
- [Table 2-3](#) Analog outputs
- [Table 2-4](#) Digital I/Os (other than host interfaces)
- [Table 2-5](#) Host digital interfaces
- [Table 2-6](#) Support circuits
- [Table 2-7](#) Do not connect pads
- [Table 2-8](#) Power supply pads
- [Table 2-9](#) Ground pads

Table 2-2 Pad descriptions – analog inputs

Pad #	Pad name	Pad type ¹	Functional description
107	AMIC1_INP	AI	Analog microphone 1 input, differential plus
99	AMIC1_INM	AI	Analog microphone 1 input, differential minus
91	AMIC2_INP	AI	Analog microphone 2 input, differential plus
92	AMIC2_INM	AI	Analog microphone 2 input, differential minus
84	AMIC3_INP	AI	Analog microphone 3 input, differential plus
85	AMIC3_INM	AI	Analog microphone 3 input, differential minus
76	AMIC4_INP	AI	Analog microphone 4 input, differential plus
77	AMIC4_INM	AI	Analog microphone 4 input, differential minus
69	AMIC5_INP	AI	Analog microphone 5 input, differential plus
70	AMIC5_INM	AI	Analog microphone 5 input, differential minus
61	AMIC6_INP	AI	Analog microphone 6 input, differential plus
54	AMIC6_INM	AI	Analog microphone 6 input, differential minus
89	MBHC_HSDet_L	AI	MBHC mechanical insertion/removal tip-detection pad
78	MBHC_HSDet_G	AI	Secondary MBHC mechanical insertion/removal ground-detection pad

1. See [Table 2-1](#) for parameter and acronym definitions.

Table 2-3 Pad descriptions – analog outputs

Pad #	Pad name	Pad type ¹	Functional description
102	EAROP	AO	Earpiece amplifier output, differential plus
110	EAROM	AO	Earpiece amplifier output, differential minus
111	HPH_L	AO	Headphone left output
103	HPH_R	AO	Headphone right output
88	HPH_REF	AI	Capless headphone ground reference of the PA
109	LINE_OUT1_P	AO	Audio line output 1, differential plus
94	LINE_OUT1_M	AO	Audio line output 1, differential minus
101	LINE_OUT2_P	AO	Audio line output 2, differential plus
86	LINE_OUT2_M	AO	Audio line output 2, differential minus
108	LINE_OUT3	AO	Audio line output 3, single-ended
100	LINE_OUT4	AO	Audio line output 4, single-ended
93	LINE_OUT_REF	AI	Audio line outputs 3 and 4 ground reference

1. See [Table 2-1](#) for parameter and acronym definitions.

Table 2-4 Pad descriptions – digital I/Os (other than host interfaces)

Pad #	Pad name	Pad type ¹	Functional description
Digital microphone (DMIC) interfaces			
50	DMIC1_DATA	DI	Data for digital microphones 1 and 2
43	DMIC1_CLK	DO	Clock for digital microphones 1 and 2
58	DMIC2_DATA	DI	Data for digital microphones 3 and 4
5	DMIC2_CLK	DO	Clock for digital microphones 3 and 4
20	DMIC3_DATA	DI	Data for digital microphones 5 and 6
36	DMIC3_CLK	DO	Clock for digital microphones 5 and 6
SoundWire port			
4	PDM_DATA	B	SoundWire data for WSA8810/WSA8815 smart speaker amplifier
11	PDM_CLK	DO	SoundWire clock for WSA8810/WSA8815 smart speaker amplifier

1. See [Table 2-1](#) for parameter and acronym definitions.

Table 2-5 Pad descriptions – host digital interfaces

Pad #	Pad name	Pad type ¹	Functional description
SLIMbus bidirectional audio			
12	SLIMBUS_DATA2	B	Bidirectional (Rx/Tx) SLIMbus data bit 2
27	SLIMBUS_DATA1	B	Bidirectional (Rx/Tx) SLIMbus data bit 1
34	SLIMBUS_CLK	B	Bidirectional (Rx/Tx) SLIMbus clock
Interintegrated circuit (I2C) port			
67	I2C_SDA	B	I ² C serial data
66	I2C_SCL	B	I ² C serial clock
I²S bus – Rx direction			
14	RX_I2S_SCK	B	I ² S bit clock, Rx direction
68	RX_I2S_WS	B	I ² S word select, Rx direction
29	RX_I2S_SD1	DI	I ² S serial data line 1, Rx direction
15	RX_I2S_SD0	DI	I ² S serial data line 0, Rx direction
I²S bus – Tx direction			
19	TX_I2S_SCK	B	I ² S bit clock, Tx direction
23	TX_I2S_WS	B	I ² S word select, Tx direction
38	TX_I2S_SD1	DO	I ² S serial data line 1, Tx direction
7	TX_I2S_SD0	DO	I ² S serial data line 0, Tx direction
Clock circuits			
71	MCLK	AI	Master clock input
72	MCLK2	AI	Master clock input 2

Table 2-5 Pad descriptions – host digital interfaces (cont.)

Pad #	Pad name	Pad type ¹	Functional description
Discrete status and control signals			
26	RESET_N	DI	WCD9335 IC-level reset
73	RF_PA_ON	DI	Indicates that GSM RF power amplifier is about to burst
41	INTR1	DO	Interrupt output 1
56	INTR2	DO	Interrupt output 2
87	MODE0	DI	Digital interface mode selection (SLIMbus or I ² S) bit 0
79	MODE1	DI	Digital interface mode selection (SLIMbus or I ² S) bit 1

1. See [Table 2-1](#) for parameter and acronym definitions.

Table 2-6 Pad descriptions – support circuits

Pad #	Pad name	Pad type ¹	Functional description
SIDO buck			
9	VSW_SIDO	AI, AO	SIDO buck switching node
31	VAUX_SIDO	AI, AO	SIDO buck auxiliary voltage node
39	VOUT_A_SIDO	AO	SIDO output voltage for analog circuits
46	VOUT_D_SIDO	AO	SIDO output voltage for digital circuits
Buck SMPS			
75	VSW_BUCK	AI, AO	Buck SMPS switching node
82	VOUT_BUCK	AO	Buck SMPS output node 1
SIMO flyback			
105	FLYBK_VNEG_OUT	AO	Flyback SIMO negative output for PAs
112	FLYBK_VNEG_DAC	AO	Flyback SIMO negative output for DACs
98	VSW_FLYBK	AI, AO	Flyback SIMO switching node
Low-dropout (LDO) linear regulator			
32	LDO_H	AO	Internal-circuitry LDO high-voltage output load capacitor
Microphone bias voltage sources			
18	MIC_BIAS1	AO	Microphone bias output voltage 1
25	MIC_BIAS2	AO	Microphone bias output voltage 2
10	MIC_BIAS3	AO	Microphone bias output voltage 3
17	MIC_BIAS4	AO	Microphone bias output voltage 4
33	MICB_CFILT_REF	AI	Microphone bias shared reference ground of the circuits
Bandgap voltage reference decoupling			
48	CCOMP	AO	Bandgap reference circuit compensation capacitor
Battery voltage monitor			
3	VBAT_ADC_IN	AI	Input to VBAT ADC

Table 2-6 Pad descriptions – support circuits (cont.)

Pad #	Pad name	Pad type ¹	Functional description
JTAG interface			
51	JTCK	DI	JTAG clock
6	JTDI	DI	JTAG data input
45	JTDO	DO	JTAG data output
44	JTMS	DI	JTAG mode select
74	JTRST	DI	JTAG reset

1. See [Table 2-1](#) for parameter and acronym definitions.

Table 2-7 Pad descriptions – do not connect pads

Pad #	Pad name	Functional description
1, 113	DNC	Do not connect; connected internally, do not connect externally

Table 2-8 Pad descriptions – power supply pads

Pad #	Pad name	Functional description
104	PA_VNEG	Negative supply for PAs
97	PA_VPOS	Positive supply for PAs
55	VDD_A_LV	Power for analog low-voltage circuits
83	VDD_BUCK	Power for buck SMPS
22, 35, 42, 52	VDD_CORE	Power for core digital circuits
13, 37	VDD_MX	Power for on-chip memory
40	VDD_MIC_BIAS	Power for the LDO and microphone bias circuits
21, 53	VDD_IO	Power for digital I/O pads
96	VDD_RX	Power for analog audio output (Rx) circuits
16	VDD_SIDO	Power for the SIDO buck
62	VDD_TX	Power for analog audio input (Tx) circuits

Table 2-9 Pad descriptions – ground pads

Pad #	Pad name	Functional description
8, 28, 30, 49, 57, 59, 60, 64, 65, 80, 81, 106	GND	Ground
90	GND_BUCK	Ground for buck SMPS circuits
63	GND_CCOMP	Ground for bandgap reference circuits
95	GND_RX	Ground for analog audio input (Rx) circuits
2, 24	GND_SIDO	Ground for SIDO buck
47	GND_TX	Ground for analog audio input (Tx) circuits

3 Electrical specifications

3.1 Absolute maximum ratings

Absolute maximum ratings (Table 3-1) reflect the worst-case conditions that WCD9335 devices are exposed to during testing. They are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance at any absolute maximum condition, or after exposure to any of these conditions, are not guaranteed or implied. Exposure can shorten the life of the device.

Table 3-1 Absolute maximum ratings

Parameter	Description	Minimum	Maximum	Units
Power supply voltages				
VDD_MIC_BIAS	Power for the LDO and microphone bias circuits	-0.30	4.80	V
VDD_RX	Power for analog audio output (Rx) circuits	-0.30	2.16	V
VDD_TX	Power for analog audio input (Tx) circuits	-0.30	2.16	V
VDD_BUCK	Power for buck SMPS	-0.30	2.16	V
VDD_SIDO	Power for the SIDO buck	-0.30	2.16	V
VDD_IO	Power for digital I/O pads	-0.30	2.16	V
VDD_A_LV	Power for analog low-voltage circuits	-0.30	1.30	V
VDD_MX	Power for on-chip memory	-0.30	1.30	V
VDD_CORE	Power for core digital circuits	-0.30	1.30	V
Signal pads				
VIN_DIG	Any digital input, nonpower	-0.30	2.15	V
VIN_ANA	Any analog input, nonpower	-0.30	2.90	V
VBAT_ADC_IN	Input to VBAT ADC	-0.30	4.80	V

3.2 Operating conditions

Operating conditions include parameters that are under the control of the design team: power supply voltage, power distribution impedances, and thermal conditions (Table 3-2). The WCD9335 meets all performance specifications listed in Section through Section 3.7.6, when used within the operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Operating conditions

Parameter	Description	Minimum	Typ	Maximum	Units
Power supply voltages					
VDD_MIC_BIAS	Power for the LDO and microphone bias circuits	3.15	3.80	4.60	V
VDD_RX	Power for analog audio output (Rx) circuits	1.70	1.80	1.90	V
VDD_TX	Power for analog audio input (Tx) circuits	1.70	1.80	1.90	V
VDD_BUCK	Power for buck SMPS	1.70	1.80	1.90	V
VDD_SIDO	Power for the SIDO buck	1.70	1.80	1.90	V
VDD_IO	Power for digital I/O pads	1.70	1.80	1.90	V
Internally generated input voltage					
VDD_A_LV	Power for analog low-voltage circuits	1.0	1.10	1.21	V
VDD_MX	Power for on-chip memory	1.0	1.10	1.21	V
VDD_CORE	Power for core digital circuits	0.88	1.10	1.21	V
Signal pads					
VBAT_ADC_IN	Input to VBAT ADC	2.50	3.80	4.60	V
Thermal condition					
Tc	Operating temperature (case)	-30	–	85	°C

3.3 DC power characteristics

3.3.1 Peak current

Table 3-3 Power supply peak current

Parameter	Conditions	Minimum	Typ	Maximum	Units
VDD_MIC_BIAS	–	–	–	15	mA
VDD_RX	–	–	–	25	mA
VDD_TX	–	–	–	25	mA
VDD_BUCK	–	–	–	650	mA
VDD_SIDO	–	–	–	200	mA
VDD_IO	Total for two pads	–	–	10	mA
VDD_A_LV	Included in VDD_SIDO	–	–	15	mA
VDD_MX	Included in VDD_SIDO, total for two pads	–	–	10	mA
VDD_CORE	Included in VDD_SIDO, total for four pads	–	–	40	mA

3.4 Digital logic characteristics

Table 3-4 Digital I/O characteristics

Parameter	Conditions	Minimum	Typ	Maximum	Units	
VIH	High-level input voltage	–	$0.65 \cdot VDDX$	–	$1.1 \cdot VDDX$	V
VIL	Low-level input voltage	–	0	–	$0.35 \cdot VDDX$	V
VOH	High-level output voltage	–	$0.90 \cdot VDDX$	–	VDDX	V
VOL	Low-level output voltage	–	0	–	$0.10 \cdot VDDX$	V
CIN	Digital input capacitance	–	–	–	5	pF

3.5 Audio inputs and Tx processing

Unless otherwise stated:

- All Tx performance parameters are measured with 1.02 kHz sine wave input signal, differential or single-ended inputs, $F_s = 48$ kHz, 24-bit data, and MCLK = 9.6 MHz or 12.288 MHz.
- SNR is measured by taking the ratio of the output level with input signal level of 0 dBV and 1.02 kHz sine wave to the output level with inputs grounded over a bandwidth of 20 Hz–20 kHz.

3.5.1 Analog input through digital serial interface

Table 3-5 specifies the performance of the following Tx path: Any analog input → pre-amp → ADC → digital serial interface.

NOTE Only hi-fi mode specification is listed. Lower power consumption modes are supported.

Table 3-5 Analog input through digital serial interface performance

Parameter	Conditions	Min	Typ	Max	Units
Microphone amplifier gain = 0 dB (minimum gain)					
Input-referred noise	A-weighted; inputs grounded; bandwidth 20 Hz–20 kHz	–	3.3	–	μVrms
SNR	A-weighted	–	109	–	dB
THD + N ratio	Analog input = 0 dBV; bandwidth 20 Hz–20 kHz	–	-103	–	dB
	Analog input = -1 dBV; bandwidth 20 Hz–20 kHz	–	-98	–	dB
	Analog input = -60 dBV; bandwidth 20 Hz–20 kHz; A-weighted	–	-50	–	dB
Microphone amplifier gain = 21 dB (typical gain)					
Input-referred noise	A-weighted; inputs grounded; bandwidth 20 Hz–20 kHz	–	0.9	–	μVrms
SNR	A-weighted	–	100	–	dB
THD + N ratio	Analog input = -21 dBV; bandwidth 20 Hz–20 kHz	–	-90	–	dB
	Analog input = -22 dBV; bandwidth 20 Hz–20 kHz	–	-90	–	dB
	Analog input = -81 dBV; bandwidth 20 Hz–20 kHz; A-weighted	–	-34	–	dB
THD	Analog input = -22 dBV; bandwidth 20 Hz–20 kHz	–	-107	–	dB
General requirements					
Absolute gain error	Hi-fi mode	–	-0.1	–	dB
Full scale input signal	Measure differential input level that gives 0 dBFS output level; gain = 0 dB	–	0.1	–	dBV
Power supply rejection (VDD_TX)	0 < f < 1 kHz; 100 mVpp sine wave imposed on the power supply; analog input = 0 Vrms Terminate inputs with 0 Ω; gain = 0 dB	–	113	–	dB
	1 kHz < f < 5 kHz; 100 mVpp sine wave imposed on the power supply; analog input = 0 Vrms Terminate inputs with 0 Ω; gain = 0 dB	–	107	–	dB
	5 kHz < f < 20 kHz; 100 mVpp sine wave imposed on the power supply; analog input = 0 Vrms Terminate inputs with 0 Ω; gain = 0 dB	–	94	–	dB
Input impedance	–	1	–	–	MΩ
Input capacitance	Analog pad	–	–	30	pF

Table 3-5 Analog input through digital serial interface performance (cont.)

Parameter	Conditions	Min	Typ	Max	Units
Rx-to-Tx crosstalk attenuation	Tx path measurement with -5 dBFS Rx path signal; separate Tx input and Rx output grounds	–	105	–	dB
Interchannel isolation	$20 < f < 20$ kHz; one input terminated with 1 k Ω and the other input gets 1 kHz at -5 dBFS. Measure the digital output of the terminated channel; separate Tx inputs grounds	–	93	–	dB

3.5.2 DMIC input through digital serial interface

Table 3-6 specifies the performance of the following Tx path:

Any digital microphone input → digital serial interface.

Table 3-6 Digital microphone input through digital serial interface performance

Parameter	Conditions	Minimum	Typ	Maximum	Units
Frequency response (from digital microphone input to SB/I²S PCM output, all sample rates)					
Frequency response	See Table 3-7 for the frequency response from digital microphone input to SB/I ² S PCM output for all the sampling rates.				

Table 3-6 Digital microphone input through digital serial interface performance (cont.)

Parameter	Conditions	Minimum	Typ	Maximum	Units
Clock rate	System clock = 9.6 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, and 48 kHz	–	600	–	kHz
	System clock = 9.6 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, and 48 kHz	–	1.2	–	MHz
	System clock = 9.6 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	2.4	–	MHz
	System clock = 9.6 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	3.2	–	MHz
	System clock = 9.6 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	4.8	–	MHz
	System clock = 12.288 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, and 48 kHz	–	768	–	kHz
	System clock = 12.288 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, and 48 kHz	–	1.536	–	MHz
	System clock = 12.288 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	2.048	–	MHz
	System clock = 12.288 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	3.072	–	MHz
	System clock = 12.288 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	4.096	–	MHz
	System clock = 12.288 MHz decimated output rates: 8 kHz, 16 kHz, 32 kHz, 48 kHz, 96 kHz, and 192 kHz	–	6.144	–	MHz
Input capacitance	–	–	1	5	pF
Board capacitance	–	–	10	50	pF

3.6 Audio outputs and Rx processing

Unless otherwise stated:

- All Rx performance parameters are measured with 1.02 kHz sine wave input signal, $F_s = 48$ kHz, 24-bit data and MCLK = 9.6 MHz or 12.288 MHz
- Receive noise is measured with no dither added to the input signal

3.6.1 Digital serial interface through earpiece analog output

Table 3-7 specifies the performance of the following Rx path: digital serial input → mono DAC → mono EAR output with 32 Ω , load unless otherwise specified.

Table 3-7 Serial interface through mono EAR output

Parameter	Conditions	Minimum	Typ	Maximum	Units
EAR output; 8/16 kHz; 16 bits					
Receive noise	A-weighted; input = -999 dBFS, 6 dB gain mode	–	8.4	–	μ Vrms
	A-weighted; input = -999 dBFS, 0 dB gain mode	–	5	–	μ Vrms
SNR	Ratio of full-scale output to output noise level, A-weighted, 6 dB gain	–	107	–	dB
THD + N ratio	PCMI = 0 dBFS, 20 Hz–20 kHz, 6 dB gain	–	-91	–	dB
	PCMI = -1 dBFS, 20 Hz–20 kHz, 6 dB gain	–	-90	–	dB
	PCMI = -60 dBFS, 20 Hz–20 kHz, 6 dB gain, A-weighted	–	-38	–	dB
EAR output; 48 kHz; 16 bits					
Receive noise	A-weighted; input = -999 dBFS, 6 dB gain mode	–	8.4	–	μ Vrms
	A-weighted; input = -999 dBFS, 0 dB gain mode	–	5	–	μ Vrms
SNR	Ratio of full-scale output to output noise level, A-weighted, 6 dB gain	–	107	–	dB
THD + N ratio	PCMI = 0 dBFS, 20 Hz–20 kHz, 6 dB gain	–	-96	–	dB
	PCMI = -1 dBFS, 20 Hz–20 kHz, 6 dB gain	–	-95	–	dB
	PCMI = -60 dBFS, 20 Hz–20 kHz, 6 dB gain, A-weighted	–	-40	–	dB
Other characteristics					
Full-scale output voltage	Input = 0 dBFS, PA gain = 6 dB	–	1.96	–	Vrms
	Input = 0 dBFS, PA gain = 0 dB	–	0.99	–	Vrms
Output power	PA gain = 6 dB, 32 Ω , THD+N \leq 1%	–	120	–	mW
Output load	Supported output load	10	32	–	Ω

Table 3-7 Serial interface through mono EAR output (cont.)

Parameter	Conditions	Minimum	Typ	Maximum	Units
Tx-to-Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal; separate Tx input and Rx output grounds	–	101	–	dB
Power supply rejection	0 < f < 1 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	101	–	dB
	1 kHz < f < 5 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	95	–	dB
	5 kHz < f < 20 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	80	–	dB
Disabled output impedance	Measured externally with the amplifier disabled	–	38	–	kΩ
Output capacitance	The differential output load capacitance that EAR PA can support including any PCB trace, EMI, ESD, and transducer capacitances.	–	–	500	pF
Output DC offset	Input = -999 dBFS, measured between differential output	–	0.73	–	mV
Turn on/off click-and-pop level	A-weighted, 6 dB gain	–	0.5	–	mVpp

3.6.2 Digital serial interface through HPH output

Table 3-8 specifies the performance of the following Rx path: digital serial input → stereo DAC → stereo Class H HPH with 16 Ω load, unless otherwise specified.

Table 3-8 Serial interface through HPH output

Parameter	Conditions	Minimum	Typ	Maximum	Units	
HPH; 48 kHz/44.1 kHz/16-bits						
Receive noise	A-weighted; input = -999 dBFS					
	Standard mode	–	0.89	–	μVrms	
	Hi-fi mode	–	0.77	–	μVrms	
	Low-power mode	–	1.04	–	μVrms	
SNR	Ratio of full-scale output to output noise level, A-weighted					
	Standard mode	–	121	–	dB	
	Hi-fi mode	–	122	–	dB	
	Low-power mode	–	119	–	dB	
THD + N ratio	PCMI = 0 dBFS; 20 Hz–20 kHz	Standard mode	–	-97	–	dB
		Hi-fi mode	–	-98	–	dB
		Low-power mode	–	-92	–	dB
	PCMI = -1 dBFS; 20 Hz–20 kHz	Standard mode	–	-96	–	dB
		Hi-fi mode	–	-97	–	dB
		Low-power mode	–	-92	–	dB
	PCMI = -60 dBFS; 20 Hz–20 kHz, A-weighted	Standard mode	–	-41	–	dB
		Hi-fi mode	–	-41	–	dB
		Low-power mode	–	-41	–	dB
HPH; 48 kHz/44.1 kHz/192 kHz/24-bits; 384 kHz/32-bits						
Receive noise	A-weighted; input = -999 dBFS					
	Standard mode	–	0.89	–	μVrms	
	Hi-fi mode	–	0.77	–	μVrms	
	Low-power mode	–	1.04	–	μVrms	
SNR	Ratio of full-scale output to the output noise level, A-weighted					
	Standard mode	–	121	–	dB	
	Hi-fi mode	–	122	–	dB	
	Low-power mode	–	119	–	dB	

Table 3-8 Serial interface through HPH output (cont.)

Parameter	Conditions	Minimum	Typ	Maximum	Units
THD + N ratio	PCMI = 0 dBFS; 20 Hz– 20 kHz Standard mode Hi-fi mode Low-power mode	–	-104	–	dB
		–	-105	–	dB
		–	-93	–	dB
	PCMI = -1 dBFS; 20 Hz– 20 kHz Standard mode Hi-fi mode Low-power mode	–	-104	–	dB
		–	-105	–	dB
		–	-95	–	dB
	PCMI = -60 dBFS; 20 Hz– 20 kHz; A-weighted Standard mode Hi-fi mode Low-power mode	–	-61	–	dB
		–	-62	–	dB
		–	-60	–	dB
Other characteristics					
Full-scale output voltage	Input = 0 dBFS; 16 Ω or 32 Ω load	–	1	–	V _{rms}
Output power	Input = 0 dBFS, 16 Ω load	–	62.5	–	mW
	Input = 0 dBFS, 32 Ω load	–	31.25	–	mW
Output load	Supported output load	4	16	–	Ω
Tx-to-Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal, separate Tx input, and the Rx output grounds	–	118	–	dB
Inter-channel isolation	Measured channel output = -999 dBFS; second DAC channel output = -5 dBFS; separate GND for HPH_L and HPH_R ■ 1 kHz ■ 20 kHz	–	105	–	dB
		–	97	–	dB
Inter-channel gain error	Delta between the left and right channels; input = 1 kHz at -20 dBFS	-0.3	–	0.3	dB
Inter-channel phase error	Delta between the left and right channels; input = 1 kHz at -20 dBFS	–	0	–	degree
Power supply rejection (VDD_RX or VDD_BUCK)	0 kHz < f < 1 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	109	–	dB
	1 kHz < f < 5 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	99	–	dB
	5 kHz < f < 20 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	77	–	dB
Disabled output impedance	Measured externally, with the amplifier disabled	–	9.2	–	Ω

Table 3-8 Serial interface through HPH output (cont.)

Parameter	Conditions	Minimum	Typ	Maximum	Units
Output capacitance	Single-ended output load capacitance that HPH PA can support including any PCB trace, EMI, ESD, and transducer capacitances	–	–	1000	pF
Output DC offset	Measured between HPH_L or HPH_R and ground	–	0	–	mV
Turn on/off click-and-pop level	A-weighted, 16 Ω , 32 Ω , or 10 k Ω load	–	–	–	–
	Standard mode	–	16	–	μ Vpp
	Class-H hi-fi mode	–	16	–	μ Vpp
	Low-power mode	–	17	–	μ Vpp

3.6.3 Digital serial interface through stereo hi-fi differential line outputs

Table 3-9 specifies the performance of the following Rx path: digital serial input \rightarrow stereo DAC \rightarrow stereo hi-fi differential line outputs with 600 Ω load on the positive output and 200 Ω load on the negative output, unless otherwise specified.

Table 3-9 Serial interface through stereo-differential line outputs

Parameter	Conditions	Minimum	Typ	Maximum	Units
Line output differential; 48 kHz/44.1 kHz/192 kHz/24 bits; 384 kHz/32-bits					
Receive noise	A-weighted; input = -999 dBFS	–	0.58	–	μ Vrms
SNR	Ratio of full-scale output to output noise level; A-weighted	–	130	–	dB
THD + N ratio	PCMI = 0 dBFS; 20 Hz–20kHz	–	-109	–	dB
	PCMI = -1 dBFS; 20 Hz–20 kHz	–	-109	–	dB
	PCMI = -60; dBFS 20 Hz–20 kHz, A-weighted	–	-70	–	dB
Other characteristics					
Full-scale output voltage	Input = 0 dBFS	–	1.97	–	Vrms
Output load	Supported output load (at each output pad)	200	–	–	Ω
Tx-to-Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz; separate Tx input and Rx output grounds	–	119	–	dB

Table 3-9 Serial interface through stereo-differential line outputs (cont.)

Parameter	Conditions	Minimum	Typ	Maximum	Units
Power supply rejection	0 kHz < f < 1 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	110	–	dB
	1 kHz < f < 5 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	102	–	dB
	5 kHz < f < 20 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	93	–	dB
Disabled output impedance	Measured externally from each pad to GND, with the amplifier disabled	–	15.2	–	Ω
Output capacitance	Differential output load capacitance that the line PA can support, including any PCB trace, EMI, ESD, and input capacitances of external circuits	–	–	100	pF
Turn on/off click and pop level	A-weighted	–	0.028	–	mVpp

3.6.4 Digital serial interface through single-ended line output

Table 3-10 specifies the performance of the following Rx path: digital serial input → stereo DAC → single-ended line output in Class-AB mode with 1 kΩ load, unless otherwise specified.

Table 3-10 Serial interface through stereo line output

Parameter	Conditions	Minimum	Typ	Maximum	Units
Line out SE; 48 kHz/44.1 kHz/16-bits					
Receive noise	A-weighted; input = -999 dBFS	–	1.16	–	μVrms
SNR	Ratio of full-scale output to output noise level, A-weighted	–	119	–	dB
THD + N ratio	PCMI = 0 dBFS; 20 Hz–20 kHz	–	-96	–	dB
	PCMI = -1 dBFS; 20 Hz–20 kHz	–	-95	–	dB
	PCMI = -60 dBFS; 20 Hz–20 kHz; A-weighted	–	-41	–	dB
Line out SE; 48 kHz/44.1 kHz/192 kHz/24-bits					
Receive noise	A-weighted; input = -999 dBFS	–	1.16	–	μVrms
SNR	Ratio of full-scale output to output noise level, A-weighted	–	119	–	dB
THD + N ratio	PCMI = 0 dBFS; 20 Hz–20 kHz	–	-99	–	dB
	PCMI = -1 dBFS; 20 Hz–20 kHz	–	-99	–	dB
	PCMI = -60 dBFS; 20 Hz–20 kHz; A-weighted	–	-59	–	dB
Other characteristics					

Table 3-10 Serial interface through stereo line output (cont.)

Parameter	Conditions	Minimum	Typ	Maximum	Units
Full-scale output voltage	Input = 0 dBFS	–	1	–	V _{rms}
Output load	Supported output load	1	–	–	kΩ
Tx-to-Rx crosstalk attenuation	Rx path measurement with -5 dBFS Tx path signal, separate Tx input, and Rx output grounds	–	114	–	dB
Inter-channel isolation	20 < f < 20 kHz, measured channel output = -999 dBFS, second DAC channel output = -5 dBFS, separate GND on line outputs	–	111	–	dB
Power supply rejection	0 kHz < f < 1 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	112	–	dB
	1 kHz < f < 5 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	100	–	dB
	5 kHz < f < 20 kHz; 100 mVpp sine wave imposed on the power supply; PCMI = -999 dBFS	–	83	–	dB
Disabled output impedance	Measured externally, with the amplifier disabled	–	14.5	–	Ω
Output capacitance	Single-ended output load capacitance that the line PA can support including any PCB trace, EMI, ESD, and input capacitances of external circuits	–	–	100	pF
Turn on/off click-and-pop level	A-weighted	–	0.2	–	mVpp

3.7 Digital I/Os and digital processing

Digital logic characteristics are defined in [Section 3.4](#). The supported industry standards are identified in the following subsections.

3.7.1 SLIMbus

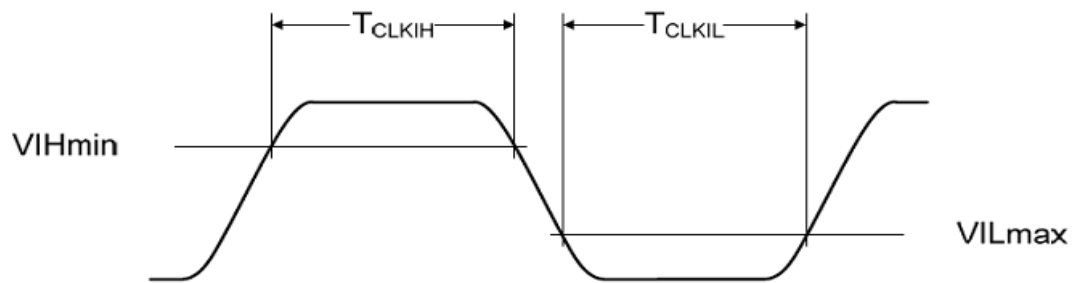


Figure 3-1 Received clock signal constraints

Table 3-11 Clock input timing requirements

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
T_{CLKIH}	CLK input high time	$I_{OL} = 1 \text{ mA}$	12	–	–	ns
V_{CLKIL}	CLK input low time	$I_{OH} = 1 \text{ mA}$	12	–	–	ns
SR_{CLKI}	Clock input slew rate	Load = 15 pF or 75 pF	$0.02 \times V_{DD}$	–	–	V/ns

Table 3-12 Data output timing characteristics

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
SR_{DATA}	Data output slew rate	$20\% < V_O < 80\%$	–	–	$0.5 \times V_{DD}$	V/ns
T_{DV}	Time for data output valid	$I_{OH} = 1 \text{ mA}$	–	–	12	ns

Table 3-13 Data input timing requirements

Symbol	Parameter	Conditions	Minimum	Typ	Maximum	Units
T_H	Data input hold time	–	2	–	–	ns
T_{SETUP}	Data input setup time	–	3	–	–	ns

NOTE The WCD9335 SLIMbus is compliant to the clock and data specifications, as specified in the *MIPI Alliance Specification for Serial Low-power Inter-chip Media Bus (SLIMbus) Version 1.01.01*.

3.7.2 Inter-IC sound (I²S)

Table 3-14 Supported I²S standards and exceptions

Applicable standards	Feature exceptions	WCD9335 variations
<i>Phillips I²S Bus Specifications</i> , revised June 5, 1996	No external controller support	None

Table 3-15 Master transmitter with data rate of 16 MHz

Parameter	Conditions	Minimum	Typ	Maximum	Unit
Clock period T	I ² S requirement: min T = 62.5	–	62.5	–	ns
Clock high t(hc)	I ² S requirement: min > 0.35 T	–	–	–	ns
Clock low t(lc)	I ² S requirement: min > 0.35 T	–	–	–	ns
Delay t(dtr)	I ² S requirement: max < 0.8 T	–	–	15.6	ns
Hold time t(htr)	I ² S requirement: min > 0	3.2	–	–	ns

Table 3-16 Slave receiver with clock rate of 16 MHz

Parameter	Conditions	Minimum	Typ	Maximum	Unit
Clock period T	I ² S requirement: min T = 62.5	–	62.5	–	ns
Clock high t(hc)	I ² S requirement: min < 0.35 T	–	–	–	ns
Clock low t(lc)	I ² S requirement: min < 0.35 T	–	–	–	ns
Setup time t(sr)	I ² S requirement: min < 0.2 T	15.6	–	–	ns
Hold time t(htr)	I ² S requirement: min < 0	0	–	–	ns

3.7.3 Inter-integrated circuit (I²C)

Table 3-17 Supported I²C standards and exceptions

Applicable standards	Feature exceptions	WCD9335 variations
<i>I²C Specification</i> , version 6.0, October 4 April 2014 (Phillips Semiconductor document number 9398 393 40011)	–	None

3.7.4 Digital microphone PDM interface

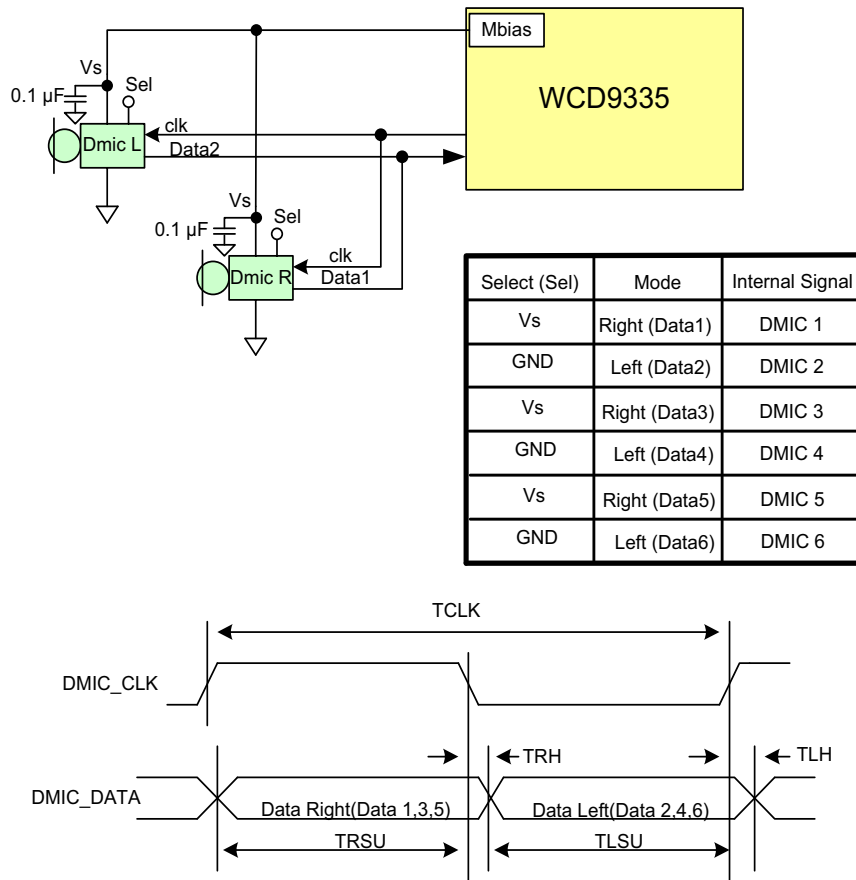


Figure 3-2 WCD9335 digital microphone PDM interface timing

Table 3-18 Digital microphone timing

Parameter	Minimum	Typ	Maximum	Unit
DMIC clock period (TCLK)	163	–	1666	ns
DMIC clock duty cycle	45	–	55	%
Data left setup time to DMIC clock rising edge (TLSU)	10	–	–	ns
Data left hold time from DMIC clock rising edge (TLH)	0	–	–	ns
Data right setup time to DMIC clock falling edge (TRSU)	10	–	–	ns
Data right hold time from DMIC clock falling edge (TRH)	0	–	–	ns

3.7.5 Master clock (MCLK)

Table 3-19 Master clock (MCLK)

Parameter	Minimum	Typ	Maximum	Units
Frequency ¹	9.6	9.6	24.576	MHz
Rise/fall time	–	10	20	ns
Duty cycle	45	50	55	%

1. The codec supports 9.6 MHz, 19.2 MHz, 12.288 MHz, or 24.576 MHz frequency.

NOTE Recommendation G.711: The nominal value recommended for the sampling rate is 8000 samples per second. The tolerance on that rate should be ± 50 ppm.

3.7.6 SoundWire

WCD9335 SoundWire PHY timing parameters as specified in [Table 3-20](#) are compliant to clock and data specifications as specified in the MIPI Alliance Specification for SoundWire Version 0.8, Revision 04. See [Figure 3-3](#) and [Figure 3-4](#).

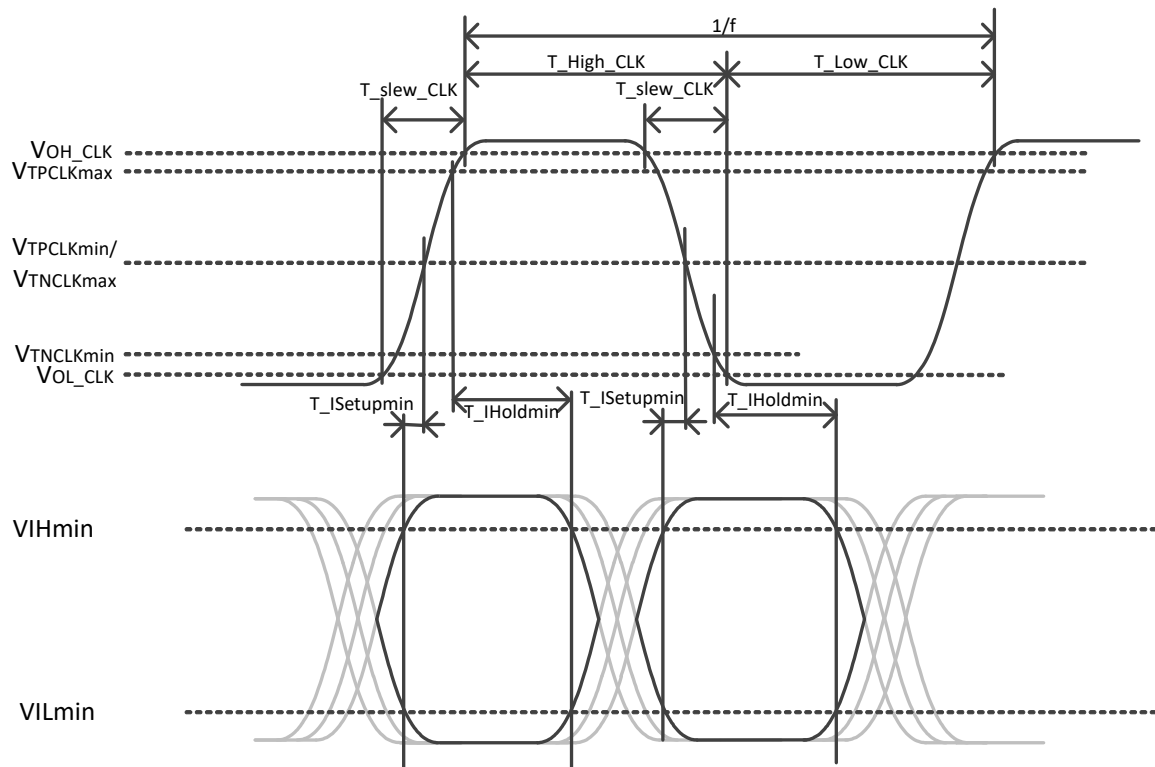


Figure 3-3 PHY timing – clock output/input and data input

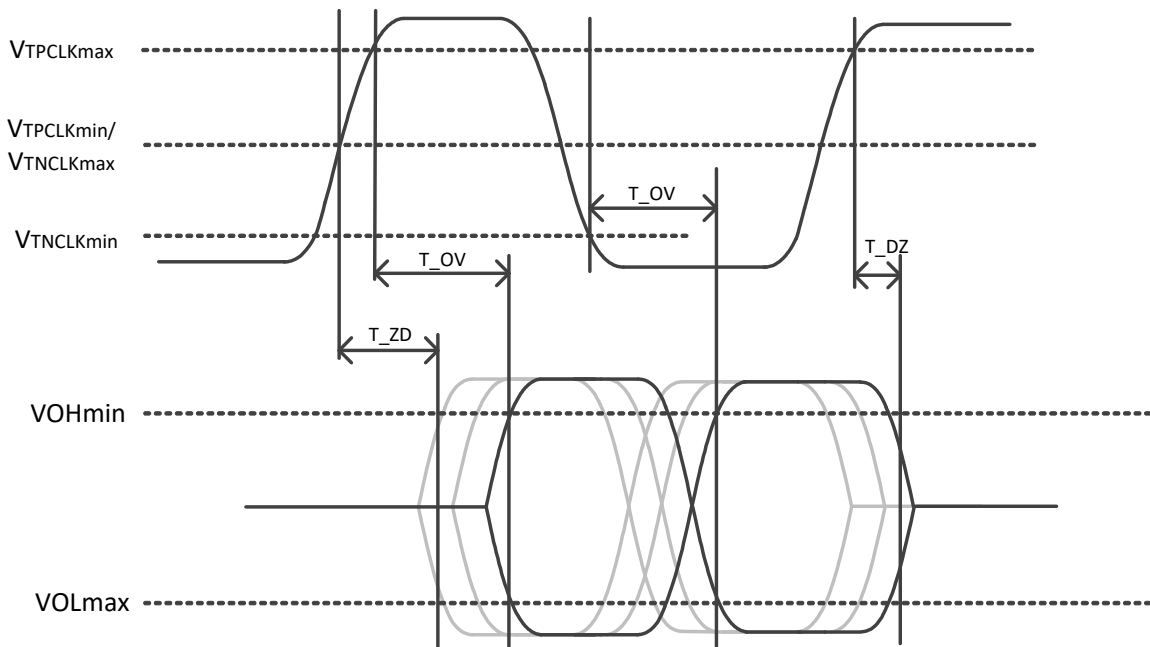


Figure 3-4 PHY timing – clock output/input and data input

Table 3-20 PHY timing parameters (1.8 V systems)

Name	Description	Minimum	Typ	Maximum	Units
VOH_CLK	Voltage level for clock high output	0.8 x VDD	–	–	V
VOL_CLK	Voltage level for clock low output	–	–	0.2 x VDD	V
VTPCLK	Voltage threshold for positive-going clock edges	0.9	–	1.17	V
VTNCLK	Voltage threshold for negative-going clock edges	0.63	–	0.9	V
T_slew_CLK	Slew time for positive or negative clock edge on clock output	2	–	5.4	ns
T_High_CLK	Duration of high half-period on clock output	35.3	–	–	ns
T_Low_CLK	Duration of low half-period on clock output	35.3	–	–	ns
DC_Out_Clock	Duty cycle generated at clock output	46	–	54	%
DC_In_Clock	Duty cycle received at clock input	45	–	55	%
T_Slew_Data	Slew time for data output changing from low to high or high to low	2	–	–	ns
T_DZ	Time to disable data output after positive or negative edge on clock input	–	–	4	ns
T_ZD	Time to enable data output after positive or negative edge on clock input	7.9	–	–	ns
T_OV	Time for data output to remain stable or valid after positive or negative edge on clock input	–	–	27.6	ns

Name	Description	Minimum	Typ	Maximum	Units
T_OH	Time for data output to remain stable after positive or negative edge on clock input	6.7	–	–	ns
t_ISetup_min	Minimum setup time demanded by a data input before a positive or negative edge on clock input	–	–	0	ns
t_IHold_min	Minimum hold time demanded by a data input after to a positive or negative edge on clock input	–	–	4	ns
t_Keeper_Settle	Time to bus-keeper generating the correct value on the data output after a continuously stable data value has been presented on the data input	–	–	2.5	ns
Frequency	Clock output frequency	0.6	– 1	12.288	MHz

1. When MCLK = 12.288 MHz, SoundWire clock = 768 kHz, 1.536 MHz, 3.072 MHz, 6.144 MHz, or 12.288 MHz.
When MCLK = 9.6 MHz, SoundWire clock = 600 kHz, 1.2 MHz, 2.4 MHz, 4.8 MHz, or 9.6 MHz.

3.8 Support circuits – analog

3.8.1 Microphone bias

NOTE Microphone bias performances are measured with 0.1 uF load capacitance and output voltage of 2.85 V.

Table 3-21 Microphone bias performance

Parameter	Conditions	Minimum	Typ	Maximum	Units
Output voltage normal operation error	3 mA microphone load	1	1.8	2.85	V
		-50	–	50	mV
Load current	Output current that the MIC bias output can source	0.005	–	6	mA
Output noise	–	–	2.5	–	µV
Power supply rejection ratio	100 mVpp applied to VDD_MIC_BIAS input; 1.5 mA microphone load				
	20 Hz	93	–	–	dB
	200 Hz to 1 kHz	113	–	–	dB
	2 kHz	100	–	–	dB
	10 kHz	90	–	–	dB
	20 kHz	78	–	–	dB
Load capacitance	Capacitances directly at the MIC bias output	0.025	0.1	0.5	µF

4 Device marking and ordering information

The WCD9335 is available in the 113 FOWPSP that includes ground pads for improved grounding, mechanical strength, and thermal continuity. The 113 FOWPSP has a $4.17 \times 3.91 \times 0.65$ mm body with a maximum height of 0.65 mm. A simplified version of the 113 FOWPSP outline drawing is shown in [Figure 4-1](#).

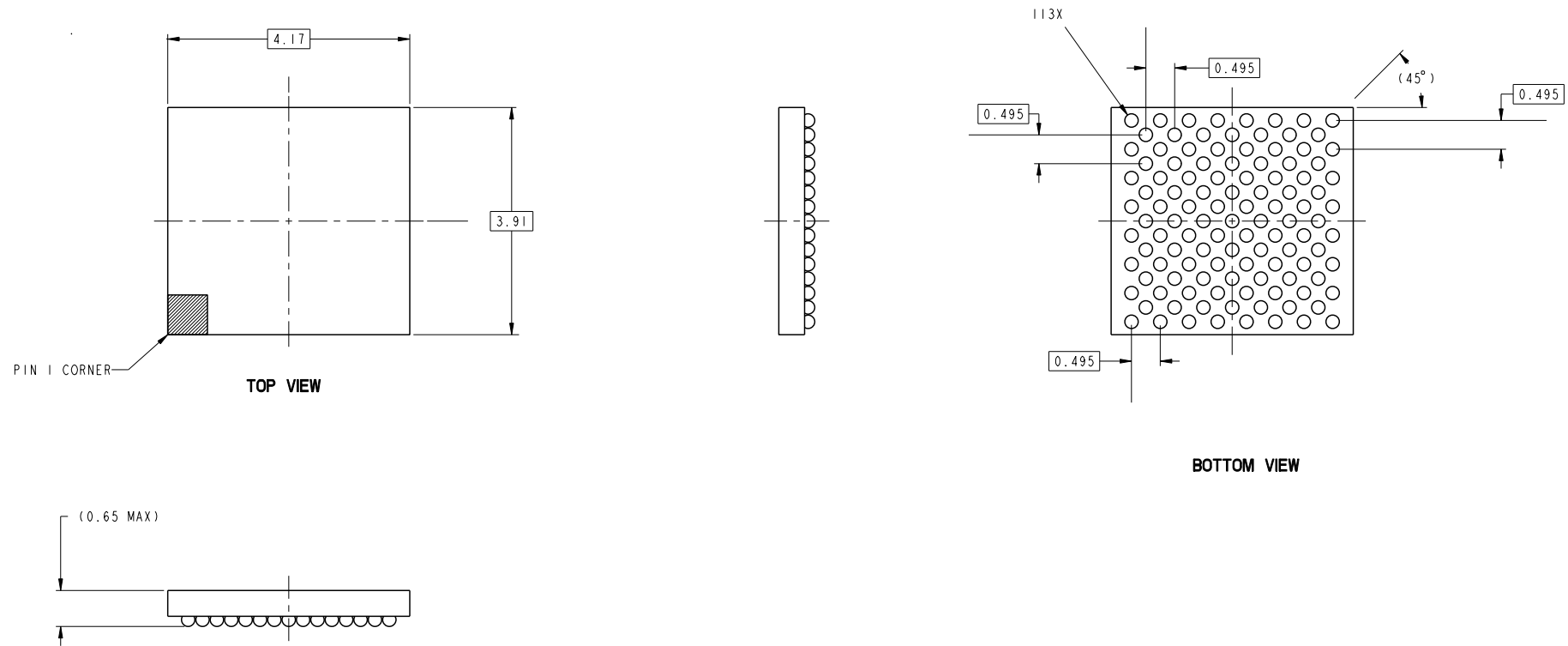


Figure 4-1 113 FOWPSP (4.17 × 3.91 × 0.65 mm) package outline drawing

NOTE This is a simplified outline drawing.

4.1 Device ordering information

4.1.1 Specification-compliant devices

Use the identification code shown in [Figure 4-2](#) to order the device.

Device ID code ▶	AAA-AAAA	— P	— CCC	DDDDDD	— EE	— RR	— S
Symbol definition ▶	Product name	Config code	Number of pads	Package type	Shipping package	Product version	Source code
Example ▶	WCD-9335	— 0	— 113	FOWPSP	— HR, SR or TR	— 03	— 0

Figure 4-2 Device identification code

5 Carrier, storage, & handling information

5.1 Carrier

5.1.1 Tape and reel information

All carrier tape systems conform to EIA-481 standards.

A simplified sketch of the WCD9335 tape carrier is shown in [Figure 5-1](#), including the proper part orientation, maximum number of devices per reel, and key dimensions.

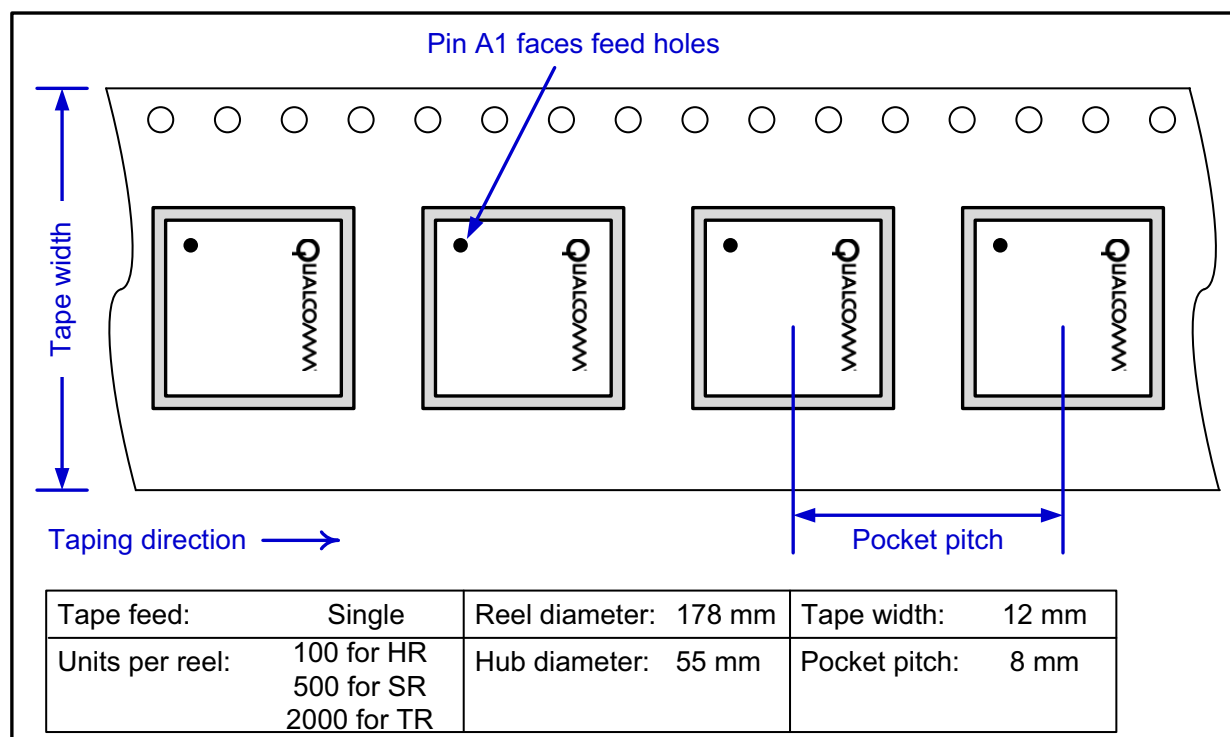


Figure 5-1 Carrier tape drawing with part orientation

Tape-handling recommendations are shown in [Figure 5-2](#).

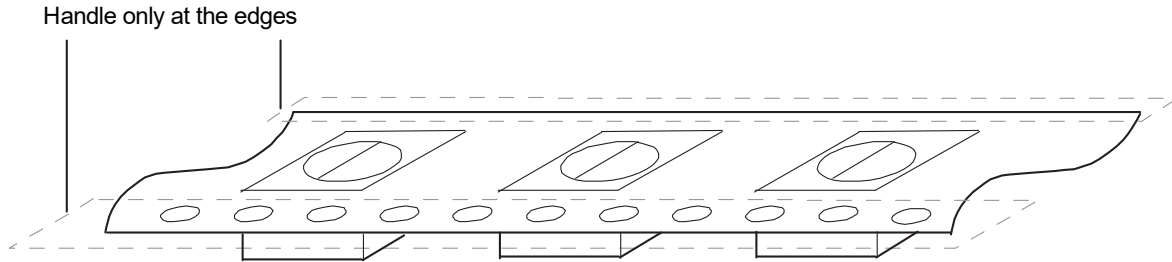


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Bagged storage conditions

The WCD9335 devices delivered in tape and reel carriers must be stored in sealed, moisture barrier, antistatic bags.

5.2.2 Out-of-bag duration

The out-of-bag duration is the time a device can be on the factory floor before being installed onto a PCB.

5.3 Handling

Tape handling was discussed in [Section 5.1.1](#). Other (IC-specific) handling guidelines are presented in this section.

Unlike traditional IC devices, the die within a fan-out wafer-level package (WLP) is not protected by an overmold and substrate; hence, these devices are relatively fragile.

NOTE To avoid damage to the die due to improper handling, follow these recommendations:

- Do not use tweezers; a vacuum tip is recommended for handling the devices.
- Carefully select a pickup tool for use during the SMT process.
- Do not touch the device when reworking or tuning the components located near the device.

5.3.1 Baking

Baking is not required if material is stored in a $\leq 30^{\circ}\text{C}/60\% \text{RH}$ condition.

5.3.2 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage can occur.

Develop and use the ESD countermeasures and handling methods to control the factory environment at each manufacturing site.

You must handle products according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

6 PCB mounting guidelines

6.1 RoHS compliance

The device complies with the requirements of the EU restriction of hazardous substances (RoHS) directive. Its tin-silver-copper (Sn/Ag/Cu) solder balls use SAC405 composition.

7 Device reliability

7.1 Reliability qualifications summary

Table 7-1 Silicon reliability results

Tests, standards, and conditions	Sample size	Result
ELFR in DPPM HTOL: JESD22-A108-A (Total samples from three different wafer lots)	370	Pass < 1000 DPPM
HTOL in FIT (I) failure in billion device hours HTOL: JESD22-A108-A (Total samples from three different wafer lots)	370	Pass < 50 FIT
Mean time to failure (MTTF) $t = 1/I$ in million hours (Total samples from three different wafer lots)	370	> 20
ESD – Human-body model (HBM) rating JESD22-A114-F (Total samples from one wafer lot)	3	2000 V
ESD – Charged-device model (CDM) rating JESD22-C101-D (Total samples from one wafer lot)	3	500 V
Latch-up (I-test): EIA/JESD78A Trigger current: ± 100 mA; temperature: 85°C (Total samples from one wafer lot)	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78A Trigger voltage: Each VDD pin, stress at $1.5 \times V_{dd}$ max per device specification; temperature: 85°C (Total samples from one wafer lot)	6	Pass

Table 7-2 Package reliability results

Tests, standards, and conditions	Assembly source SCS Sample size	Assembly source Nanium Sample size	Result
Moisture resistance test (MRT): J-STD-020E Reflow at 260 +0/-5°C (Total samples from three different assembly lots at each SAT)	480	480	Pass
Temperature cycle: JESD22-A104-D Temperature: -55°C to 125°C; number of cycles: 1000 Soak time at minimum/maximum temperature: 8–10 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-F MSL1, reflow temperature: 260°C+0/-5°C (Total samples from three different assembly lots at each SAT)	240	240	Pass
Unbiased highly accelerated stress test (UHAST): JESD22-A118-B Stress condition: 130°C/85% RH, 96 hrs Preconditioning: JESD22-A113-F MSL: 1, reflow temperature: 260 +0/-5°C (Total samples from three different assembly lots at each SAT)	240	240	Pass
High-temperature storage life: JESD22-A103-C Temperature 150°C, 1000 hours (Total samples from three different assembly lots at each SAT)	240	240	Pass
Solder ball shear: JESD22-B117	15	15	Pass
Flammability UL-STD-94 Flammability test – not required Note: ICs are exempt from flammability requirements due to their size per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which ICs are mounted are rated V-0 (better than V-1).	–	–	See Note
Physical dimensions: JESD22-B100-A Case outline drawing: Qualcomm internal document (Total samples from three different assembly lots at each SAT)	60	60	Pass

EXHIBIT 1

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