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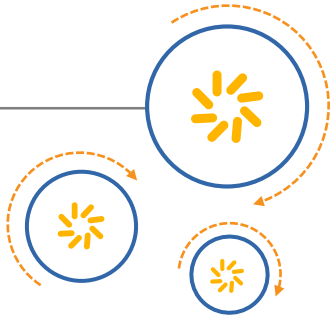

WGR7640 GNSS RF Receiver

IC Device Specification

July 2015

Qualcomm Technologies, Inc.
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LM80-P0436-31 Rev. A

Revision history

Revision	Date	Description
A	July 29, 2015	Initial release

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1 Overview

1.1 Documentation overview

This document contains a description of the chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE: Enabling some features may require additional licensing fees.

This document is part of a set of documents that describes the WGR7640 RF integrated circuits (IC) and how best to use them. The WGR7640 IC is a dedicated global navigation satellite services (GNSS) radio frequency (RF) receiver.

Technical information for these devices is primarily covered by the documents listed in Table 1-1, and all documents should be studied for a thorough understanding of the device and its applications.

Table 1-1 WGR7640 IC documents

Document number	Title and description
LM80-P0436-31 (this document)	*WGR7640 GNSS RF Receiver IC Device Specification* Provides all the WGR7640 device electrical and mechanical specifications. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
LM80-P0436-30	*WGR7640 IC Device Revision Guide* Provides a history of WGR7640 device revisions. This document explains how to identify the various device revisions, and discusses known issues (or bugs) for each revision and how to work around them
LM80-P0436-29	*WGR7640 IC GNSS RF Receiver Design Guidelines* Provides detailed descriptions of all WGR7640 IC functions and interfaces, including its various operating modes. Example applications are presented first, and then specific design topics such as layout guidelines, power-distribution recommendations, external-component recommendations, and troubleshooting techniques are addressed.

This WGR7640 IC specification is organized as follows:

Chapter 1 Provides an overview of WGR7640 IC documentation, gives a high-level functional description of the WGR7640 ICs, describes device features, and lists terms and acronyms used throughout this document.

Chapter 2 Defines the IC pin assignments.

Chapter 3 Defines the IC electrical performance specifications, including absolute maximum ratings and recommended operating conditions.

Chapter 4 Provides the visible markings and ordering information for the WGR7640 device.

Chapter 5 Describes the physical dimensions and the tape and reel packaging of the WGR7640 device.

Chapter 6 Provides specifications for mounting WGR7640 IC parts.

Chapter 7 Presents WGR7640 IC reliability data, including definition of the qualification samples and a summary of qualification test results.

1.2 WGR7640 IC introduction

The WGR7640 IC is a highly integrated RF complementary metal oxide semiconductor (CMOS) receiver IC.

Key WGR7640 functions include:

- GNSS receiver input for GPS, GLONASS, COMPASS operation
- GNSS RF-to-baseband quadrature downconverter
- An analog GNSS baseband interface to the baseband device
- GNSS Rx local oscillator (LO) source
- Voltage-controlled oscillator (VCO) and phase lock loop (PLL) circuits that support GNSS operating bands
- Option to support an external low-noise amplifer (LNA)
- Low operating voltages save battery current and allows the WLP GPS receiver (WGR) IC power to be supplied by the power management integrated circuit's (PMIC) switched-mode power supply (SMPS) circuits
- singlewire serial bus interface (SSBI) for efficient initialization, status, and control

The WGR7640 device is fabricated using an advanced RF CMOS process that accommodates high-frequency, high-precision analog circuits and low-power CMOS functions. Designed to operate with low-voltage power supplies, they are compatible with single-cell Li-Ion batteries.

This device is available in the 17-pin wafer-level nanoscale package (17 WLNSP) and is supplemented by a processor IC, such as the APQ8094, to create a GNSS receiver solution that reduces part count and printed circuit board (PCB) area.

The functional block diagram for the WGR7640 IC is shown in Figure 1-1. Major WGR7640 IC functional blocks are described in Section 1.3.

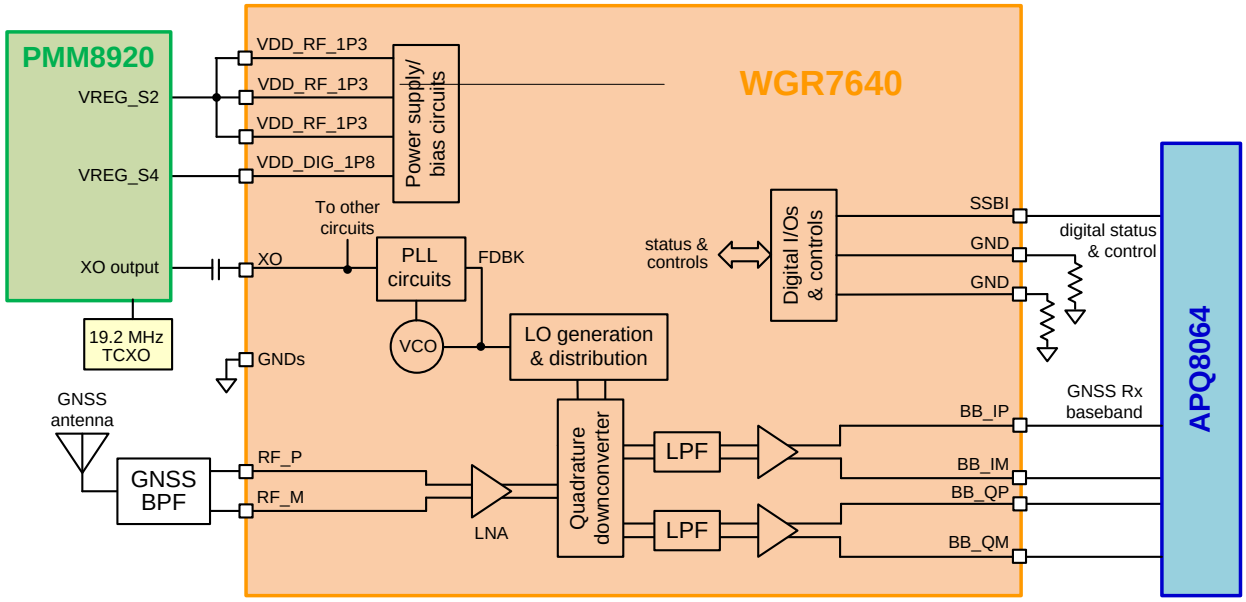

Figure 1-1 WGR7640 IC functional block diagram and example application

1.3 WGR7640 IC features

1.3.1 WGR7640 IC GNSS receive path

The WGR7640 IC GNSS input path is followed by a dedicated downconverter. The GNSS downconverter output drives a single set of baseband filters. The baseband analog output (in-phase and quadrature differential signals) are fed to the GNSS analog-to-digital converter (ADC) on the application-only processor – Qualcomm (APQ) device. The digital I/Q output of the APQ ADC goes to the GNSS engine for further processing.

1.3.2 WGR7640 IC LO generation and distribution circuits

The integrated local oscillator (LO) generation and distribution circuits are driven by internal VCOs to support various modes to yield highly flexible quadrature LO outputs to the GNSS downconverter. With the help of these LO generation and distribution circuits, it is possible to translate the signal from the RF to the baseband.

The WGR7640 IC has a dedicated synthesizer used for GNSS operation. This synthesizer provides the LO for the GNSS receiver.

For the WGR7640 IC, an external 19.2 MHz input signal obtained from the power management IC (PMIC) device is required to provide the synthesizer frequency reference to which the PLL is phase- and frequency-locked.

The WGR7640 IC integrates all of the phase-locked loop (PLL) filter components on-chip. With the integrated PLL synthesizers, the WGR7640 IC has the advantage of more flexible loop bandwidth control, fast lock time, and low integrated phase error.

1.3.3 WGR7640 IC digital interfaces

Most control and status commands are communicated through the WGR7640 IC single-line serial bus interface (SSBI), which enables efficient initialization, control of device operating modes and parameters, verification of programmed parameters, and frequency lock status reports. The baseband device SSBI controller is master while the WGR7640 IC is the slave.

1.3.4 Package features

- 17-pin wafer-level nanoscale package (17 WLNSP)
- 2.07 × 1.51 × 0.63 mm outline
- 0.4 mm pitch
- Many ground pins for better electrical grounding, mechanical strength, and thermal continuity

1.4 Summary of key WGR7640 IC features

Table 1-2 Key WGR7640 IC features

Feature	WGR7640 capability
GNSS – supported modes	Standalone, GPS, GLONASS, COMPASS
Integrated GNSS RF receiver	Dedicated circuits support GPS, GLONASS, and COMPASS
SSBI	Efficient initialization, status, and control
External LNA	Optional
Fabrication technology	65 nm RF CMOS
Small, thermally efficient package	17 WLNSP: 2.07 × 1.51 × 0.63 mm; 0.4 mm pitch

1.5 Terms and acronyms

A summary of terms and acronyms used within this document is provided for the reader's convenience.

Table 1-3 Terms and acronyms

Term or acronym	Definition
ADC	Analog to digital converter
AGC	Automatic gain control
API	Application programming interface
APQ	Application-only processor
CDM	Charge-device model
CMOS	Complementary metal oxide semiconductor
CP	Charge pump
FAQ	Fast acquisition
GNSS	Global navigation satellite services
HBM	Human-body model

Term or acronym	Definition
IC	Integrated circuit
I/Q	In-phase/quadrature-phase
LIF	Low-IF
LNA	Low-noise amplifier
LO	Local oscillator
PCB	Printed circuit board
PLL	Phase-locked loop
PM	Power management
PMIC	Power management IC
QCA	Qualcomm Atheros
RF	Radio frequency
SMPS	Switched-mode power supplies
SSBI	Single-wired serial bus interface
VCO	Voltage-controlled oscillator
VCTCXO	Voltage-controlled temperature-compensated crystal oscillator. Referred to as TCXO in this document.
WGR	WLP GPS Receiver
WLNSP	Wafer-level nanoscale package

2 Pin Definitions

The highly integrated WGR7640 device is available in the 17 WLNSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

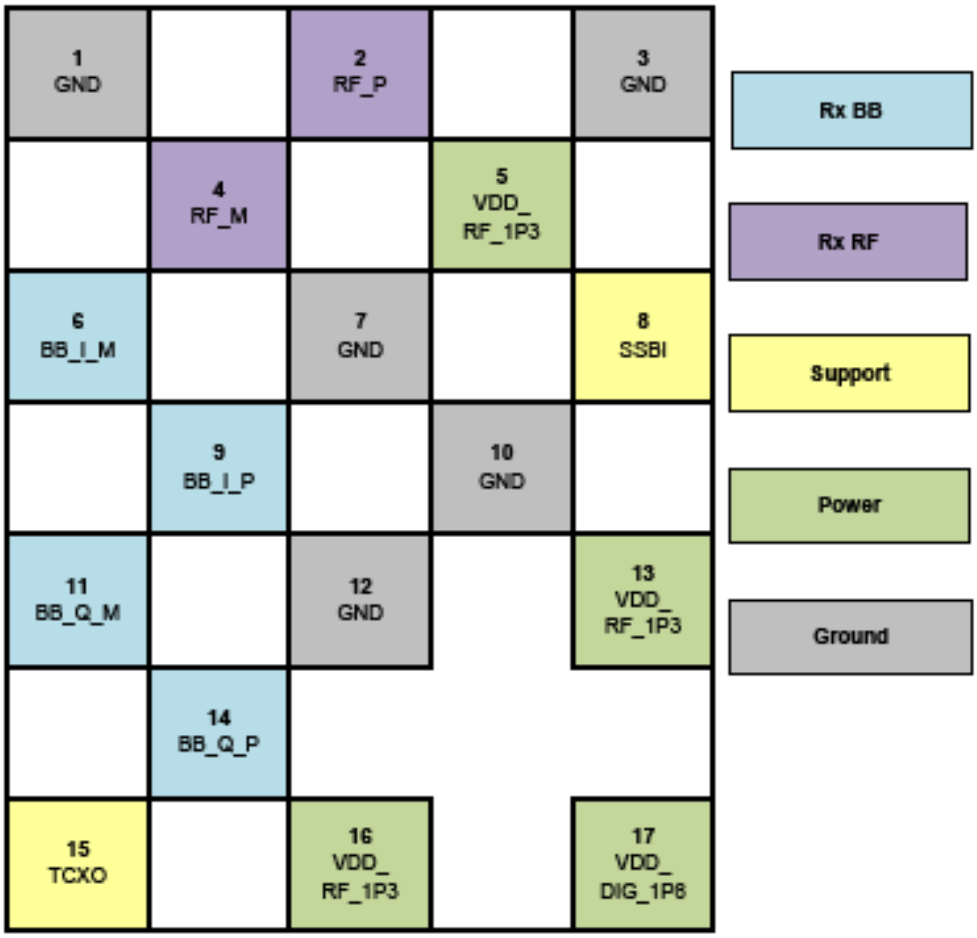

Figure 2-1 WGR7640 IC pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)

2.2 Pin descriptions

WGR7640 pins are grouped according to their functionality and are described below. Each functional grouping is presented in its own table:

Table 2-2, Receiver RF

Table 2-3, Receiver baseband

Table 2-4, Support functions

Table 2-5, Power supply pins

Table 2-6, Ground pins

Table 2-2 Receiver RF pin descriptions

Pin number	Pin name	Pin type*	Functional description
2	RF_P	AI	GNSS LNA input, plus
4	RF_M	AI	GNSS LNA input, minus

* Pin type acronyms are defined in Table 2-1.

Table 2-3 Receiver baseband pin descriptions

Pin number	Pin name	Pin type*	Functional description
6	BB_I_M	AO	GNSS receiver baseband in-phase output, minus
9	BB_I_P	AO	GNSS receiver baseband in-phase output, plus
11	BB_Q_M	AO	GNSS receiver baseband quadrature output, minus
14	BB_Q_P	AO	GNSS receiver baseband quadrature output, plus

* Pin type acronyms are defined in Table 2-1.

Table 2-4 Support functions pin descriptions

Pin number	Pin name	Pin type*	Functional description
8	SSBI	DI, DO	Single-wire serial bus interface for GNSS functions
15	TCXO	AI	19.2 MHz reference clock input

* Pin type acronyms are defined in Table 2-1.

Table 2-5 Power pins

Pin number	Pin name	Description
5	VDD_RF_1P3	Power for GNSS analog circuits
13	VDD_RF_1P3	Power for GNSS analog circuits
16	VDD_RF_1P3	Power for GNSS analog circuits
17	VDD_DIG_1P8	Power for GNSS digital circuits

Table 2-6 Ground pins

Pin numbers	Pin name	Description
1. 3, 7, 10, 12	GND	Ground

3 Electrical Specifications

3.1 WGR7640 IC absolute maximum ratings

Operating WGR7640 ICs under conditions beyond their absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating range. Functional operation and specification compliance under any absolute maximum rating condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter		Min	Typ	Max	Unit
Power supply voltages					
$V_{DD\_DIG\_1P8}$	Power for digital circuits	-0.50	–	1.91	V
$V_{DD\_X\_1P3}$ [1]	Power for analog circuits	-0.50	–	1.38	V
Signal pins					
V_{IN} [2]	Voltage on any nonpower input or output supply pin	-0.50	–	V_{DDX}	V
ESD protection – see Chapter 7					
Thermal conditions – see Chapter 4					

[1] 'X' represents the remaining characters in the pin name; see Table 2-5 for the complete VDD pin names
[2] V_{DD}X is the supply voltage associated with the input or output pin to which the test voltage is applied.

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user – power supply voltage and ambient temperature (Table 3-2). The WGR7640 ICs meet all performance specifications listed in Section 3.3 through Section 3.6 and their subsections when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded).

Table 3-2 Recommended operating conditions

Parameter		Min	Typ	Max	Units
Power supply voltages					
$V_{DD\_DIG\_1P8}$	Power for digital circuits	1.70	1.80	1.91	V
$V_{DD\_X\_1P3}$ [3]	Power for analog circuits	1.22	1.225	1.38	V
Thermal condition					
T_C	Case operating temperature	-30	+25	+85	°C

3.3 DC power characteristics

3.3.1 Average operating current

Table 3-3 Average operating current

Mode	Without ELNA	With ELNA	Units
WGR7640 1.3 V total	22.70	17.20	mA
WGR7640 1.8 V total	0.15	0.15	mA

NOTE: The above current consumption numbers are typical measured values for GPS and GLONASS; and do not include Beidou.

3.4 Digital logic characteristics

NOTE: Information listed in this section is preliminary and is subject to change.

Table 3-4 Digital I/O characteristics

Parameter		Comments[4]	Min	Max	Unit
V_{IH}	High-level input voltage		0.65 * V_{DDX}	1.91	V
V_{IL}	Low-level input voltage		0	0.35 * V_{DDX}	V
I_{IL}	Input low leakage current	V_{DDX} = maximum V_{in} = 0 to V_{DDX}	-1	1	µA
V_{OH}	High-level output voltage	V_{DDX} = minimum	V_{DDX} - 0.45	1.91	V

[3] 'X' represents the remaining characters in the pin name; see Table 2-5 for the complete VDD pin name.

[4] V_{DDX} is the supply voltage associated with the digital I/O pin being tested (connected to VDD_DIG_1P8 pin.

Parameter		Comments[4]	Min	Max	Unit
V_{OL}	Low-level output voltage	V_{DDX} = maximum	0	0.45	V
C_{in-d}	Input capacitance (digital inputs)		15	10	pF
C_{l-d}	Load capacitance (digital outputs)		15	10	pF

3.5 Support functions

Most performance specifications pertaining to support functions are simply the digital I/O characteristics listed in Table 3-4. One analog function warrants specification: the frequency reference input to on-chip clock circuits.

The RF transceiver circuits require a 19.2 MHz reference signal that is generated by the PMIC and applied to the WGR device's TCXO pin; this pin's input characteristics are listed in Table 3-5.

Table 3-5 TCXO input performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Input frequency range	19.2 MHz signal is required.	–	19.2	–	MHz
Input impedance Resistance Capacitance		 – –	 2.5 3	 – –	 kΩ pF
Input amplitude		0.8	–	1.8	V_{pp}

3.6 GNSS receiver performance

The GNSS receiver supports GPS and GLONASS – with and without an external LNA (ELNA). Pertinent specifications are given in Table 3-6. The goal for QCA is to support the design without external GNSS LNA. QCA recommends an external GNSS LNA as a backup option.

Table 3-6 GNSS receiver performance specifications

Parameter	Comments	Min	Typ	Max	Unit
Common specs (with and without ELNA)					
Input VSWR (in-band)	50 Ω with external match	–	–	2.0:1	–
Input frequency GPS GLONASS	 Center frequency (FC) = 'L1' Center frequency (FC) = 1602 MHz	 1574.42 1598	 – –	 1576.42 1606	 MHz MHz
Output load capacitance	I and Q, each single ended	–	–	20	pF
Without ELNA					
Voltage conversion gain		68	70	72	dB
Noise figure High linearity mode Low power mode	Using 0402 inductors (Q > 27) for input matching	 – –	 2.0 1.8	 3.2 3.0	 dB dB

Parameter	Comments	Min	Typ	Max	Unit
Input IP3					
High linearity mode	J1 = -20 @ FC + 138; J2 = -68 @ FC + 275.8*	-2.5	-1.0	–	dBm
Low power mode	J1 = -43 @ FC + 138; J2 = -68 @ FC + 275.8*	-9.0	-5.0	–	dBm
Input IP2					
High linearity mode	J1 = -23 @ FC + 135; J2 = -46 @ FC + 135.2*	+81	+92	–	dBm
Low power mode	J1 = -46 @ FC + 135; J2 = -46 @ FC + 135.2*	+48	+78	–	dBm
With ELNA (optional)					
Voltage conversion gain		51	53	55	dB
Noise figure	Using 0402 inductors (Q > 27) for input matching	–	3.0	4.0	dB
Input IP3	J1 = -43 @ FC + 138; J2 = -59 @ FC + 275.8*	-9.0	-3.0	–	dBm
Input IP2	J1 = -46 @ FC + 135; J2 = -46 @ FC + 135.2*	+48	+66	–	dBm

* Jammer levels have units of dBm; frequency offsets from center frequency (FC) have units of MHz.

4 Mechanical Information

4.1 Device physical dimensions

The WGR7640 is available in the 17-pin wafer-level nanoscale package (17 WLNSP) that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 17 WLNSP has a 2.07 mm by 1.51 mm body with a maximum height of 0.63 mm. Pin 1 is located by an indicator mark on the top of the package and by the ball pattern when viewed from below.

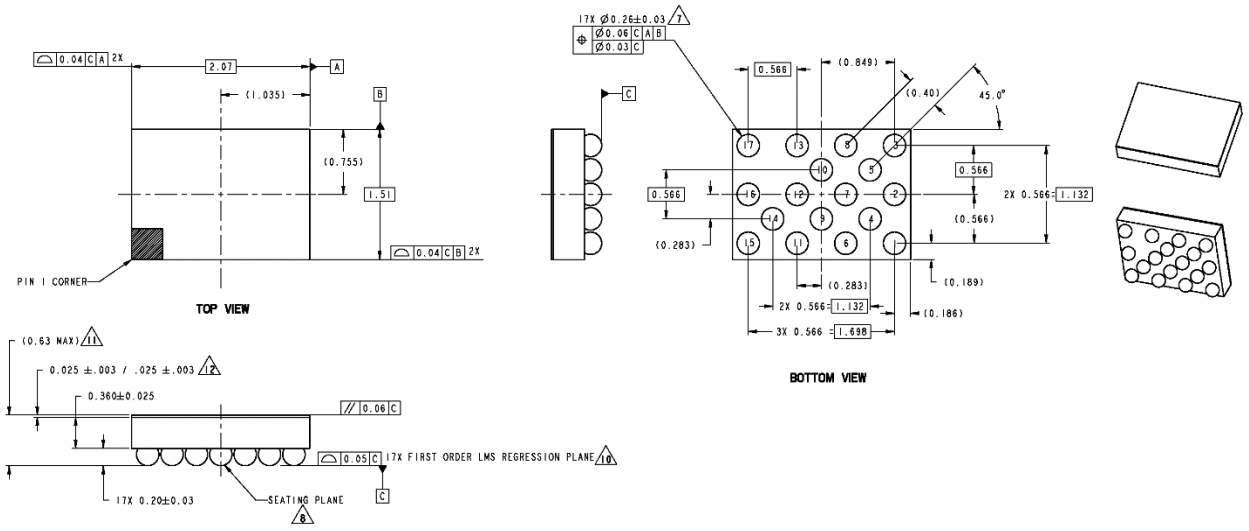

Figure 4-1 17 WLNSP outline drawing

4.2 Part marking

Figure 4-2 WGR7640 part marking (top view – not to scale)

Table 4-1 Part marking line descriptions

Line	Marking	Description
1	XXXXXXXX	XXXXXXXX = traceability number
2	FIIR##	F = supply source code ▪ F = A for TSMC II = item identifier ▪ See Table 4-2 for assigned values R = product revision – also indicates hardware ID value ▪ See Table 4-2 for assigned values ## = 2 digit wafer number

Table 4-2 Device identification code details

WGR variant	II value	R value
ES1 type		
WGR7640	03	1
CS type		
WGR7640	03	2

NOTE: For complete marking definitions of all WGR7640 IC variants and revisions, refer to the *WGR7640 IC Device Revision Guide* (LM80-NT441-13).

4.3 Device ordering information

This device can be ordered using the identification code shown in Figure 4-3 and explained below.

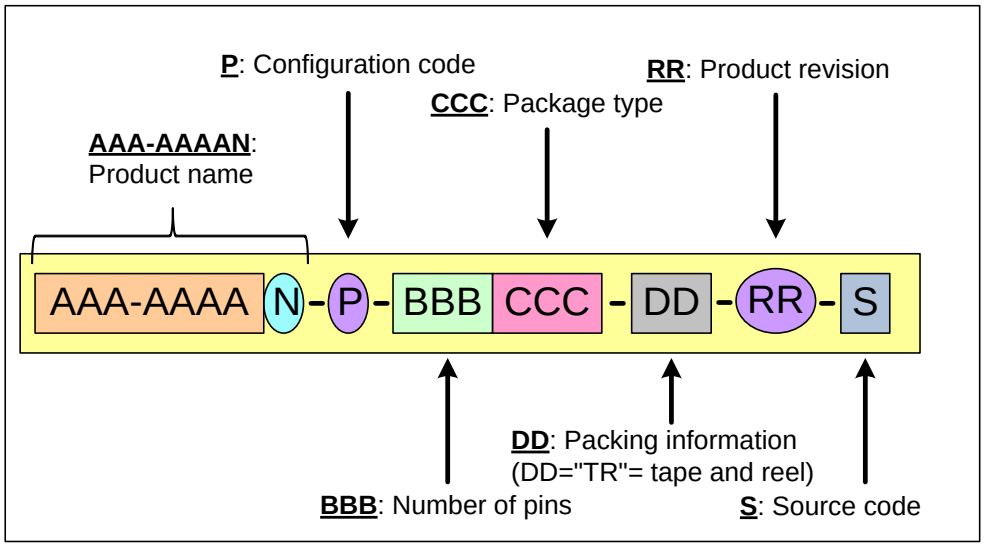

Figure 4-3 Device identification code

The product revision code (R) reflects only die revisions. A source configuration code (S) has been added to reflect all qualified sourcing combinations (i.e., multiple F codes).

An example can be as follows: WGR-7640-0-17WLNSP-TR-00-0.

Device ordering information details for all samples available to date are summarized in Section 4.3.

4.4 Device moisture-sensitivity level

Plastic-encapsulated surface mount packages are susceptible to damage induced by absorbed moisture and high temperature. The latest IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification is followed. ***The WGR7640 devices are classified as MSL 1 at 260ºC.*** This is the MSL classification temperature, which is defined as the minimum temperature of moisture sensitivity testing during device qualification.

Additional MSL information is included in:

- Section 5.2 – Storage
- Section 5.2.3 – Handling
- Section 7.1 – Reliability qualifications summary

4.5 Thermal characteristics

The WGR7640 device has typical thermal resistances as listed in Table 4-3.

Table 4-3 Device thermal resistance[5]

Parameter		Comments	Typ	Unit
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air)[6]	69.4	°C/W
θ_{JC}	Thermal resistance, J-to-C	Junction-to-case[7]	19.39	°C/W

[5]Thermal resistance values vary with die power dissipation. The specified values are calculated using a power dissipation estimate of 33 mW for the RF CMOS die.

[6]Junction-to-ambient thermal resistancε (qJA) is calculated based upon the maximum die junction temperature and the total package power dissipation; ambient temperature is 20°C.

[7]Junction-to-case thermal resistancε (qJC) applies to situations in which nearly all the heat flows out the top of the package.

5 Carrier, Storage, and Handling Information

Information about the shipping carrier and storing and handling information for the WGR7640 IC is presented in this chapter.

5.1 Carrier

5.1.1 Tape and reel information

The single-feed tape carrier for the WGR7640 device is 8 mm and the parts are placed on the tape with a 4 mm pitch. The reels are 330 mm (13 inches) in diameter with 178 mm (7-inch) hubs. Each reel can contain up to 5000 devices.

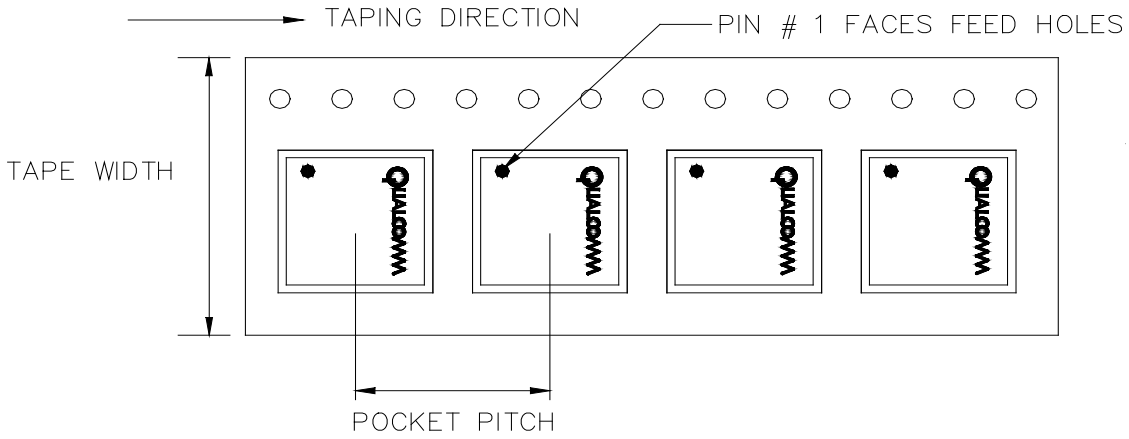

Figure 5-1 Carrier tape drawing with part orientation

The carrier tape and reel features conform to the EIA-481 standard:

- 8 mm through 200 mm embossed carrier taping
- 8 mm or 12 mm punched carrier taping of the surface mount components for automatic handling

Tape-handling recommendations are shown in Figure 5-2.

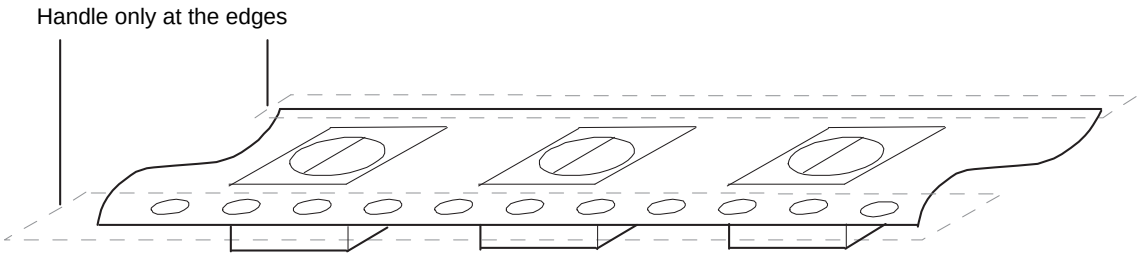

Figure 5-2 Tape handling

5.2 Storage

5.2.1 Storage conditions

The WGR7640 devices, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier, anti-static bags. The calculated shelf life in a sealed moisture bag is 60 months; this value requires an ambient temperature less than 40°C and relative humidity less than 90%.

The following shipping and storage conditions for the WLNSP reel inside the sealed bag are recommended:

- Relative humidity between 15% and 70%
- Temperature – room temperature lower than 30°C
- Atmosphere – a nitrogen dry cabinet is highly preferred

5.2.2 Out-of-bag duration

The factory floor life of when the WGR7640 IC must be soldered to a PCB does not depend upon the opening of the moisture barrier bag (MBB).

NOTE: The factory must provide an ambient temperature less than 30°C and relative humidity less than 60%, as specified in the IPC/JEDEC J-STD-033 standard.

5.2.3 Handling

Tape handling was discussed in Section 5.1.1. Other handling guidelines are presented below.

5.2.3.1 Tools and PCB rework

- Do not use hard-tip tweezers, as they may damage the WLNSP. A vacuum tip to handle the WLNSP is recommended.
- Carefully select the appropriate pickup tool to avoid any damage during the SMT process.
- Proceed with caution when reworking or tuning components that are near the WLNSP.

5.2.4 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage may result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

This product must be handled according to the ESD Association standard: ANSI/ESD S20.20-1999, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the WGR7640 device ESD ratings.

6 PCB Mounting Guidelines

6.1 Land pad and stencil design

The land pattern and stencil recommendations are based upon characterizations using lead-free solder pastes on a eight-layer test PCB and a 100 micron-thick stencil. The PCB land pattern size and stencil design for the 17 WLNSP are the same for either NSMD or SMD PCB pads.

6.2 Daisy-chain interconnect drawing

Daisy-chain packages use the same processes and materials as actual products. The daisy-chain interconnect drawing shows how packages should be attached to a characterization PCB. All SMT development described in the following section can be performed using daisy-chain packages. A bias can be applied, and solder-joint resistance can be monitored.

6.3 SMT development and characterization

The information presented in this section describes board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended to be a specification for customer SMT processes.

Characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards, which may include:

- Bend cycle
- Drop shock
- Temperature cycling
- Cyclic bend

Characterizing the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile **prior to PCB production** is recommended. Review the land pattern and stencil pattern design recommendations in Section 6.1 as a guide for characterization.

Optimizing the solder stencil pattern design and print process is critical to ensure print uniformity, decrease voiding, and increase board-level reliability.

Reflow profile conditions typically used for lead-free systems are shown in Table 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Lead-free (high-temp) condition limits
Preheat	Initial ramp	3°C/sec max
Soak	Dry out and flux activation	150°C to 190°C 60 to 75 sec
Ramp	Transition from soak to reflow	190°C to 220°C < 30 sec
Reflow	Time above solder paste melting point	50 to 70 sec
	SMT peak package body temperature	245°C
Cool down	Cool rate – ramp to ambient	6°C/sec max

6.4 SMT peak package body temperature

Factory floor-life prior to solder-attach is addressed within Section 5.2.2, Out-of-bag duration.

The following limits during the SMT board-level solder attach process are recommended:

- SMT peak package body temperature of 250°C – the temperature that should not be exceeded as measured on the package body's top surface
- Maximum duration of 40 seconds at this temperature

Although the solder paste manufacturers' recommendations for optimum temperature and duration for solder reflow should be followed, the recommended limits must not be exceeded.

6.5 SMT process verification

Verification of the SMT process prior to high-volume PCB fabrication is recommended, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

7 Part Reliability

7.1 Reliability qualifications summary

Table 7-1 WGR7640 reliability evaluation

Tests, standards, and conditions	Sample size	Results
Average failure rate (AFR) in FIT (λ); failure in billion device-hours HTOL: JESD22-A108-C Use conditions: temperature: 55°C, voltage: 1.3 V	623	22 FIT
Mean time to failure (MTTF); t = 1/ λ in million hours	623	45 Mhrs
ESD – human-body model (HBM) rating JESD22-A114-B	3	2000 V
ESD – charge-device model (CDM) rating JESD22-C101-C	3	500 V
Latch-up (I test): EIA/JESD78A Trigger current: ±100 mA Temperature = 85°C	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78 Trigger voltage: 2.07 V Temperature: 85°C	6	Pass
Moisture resistance test (MRT): J-STD-020D.01 Reflow @ 260 +0/-5°C	480	MSL1
Temperature cycle: JESD22-A104-C Temperature: -55 to 125°C Number of cycles: 1000 Soak time at min/max temperature: 5 minutes Cycle rate: 2 cycles per hour (CPH) Preconditioning: JESD22-A113-E MSL: 1; reflow temperature: 260°C	240	Pass
Unbiased highly accelerated stress test (UHAST) JESD22-A118; time = 96 hours Preconditioning: JESD22-A113-E MSL: 1; reflow temperature: 260°C	240	Pass

Tests, standards, and conditions	Sample size	Results
High-temperature storage life: JESD22-A103-C Temperature = 150°C; time = 1000 hours	240	Pass
Flammability: UL-STD-94 Flammability test – not required		See note 1
Solder ball shear: JESD22-B117	15	Pass

Note:
1. WGR7640 ICs are exempt from the flammability requirements due to their sizes, per UL/EN 60950-1, as long as they are mounted on materials rated V-1 or better. Most PWBs onto which QCA ICs are mounted are rated V-0 (which is better than V-1).

7.2 Qualification sample description

Device characteristics

- Device name: WGR7640
- Package type: 17 WLNSP
- Package body size: 2.07 mm × 1.51 mm × 0.63 mm
- Lead count: 17
- Lead composition: SAC405
- Process: 65 nm RF CMOS
- Fab sites: TSMC F12
- Assembly sites: TSMC
- Solder ball pitch: 0.4 mm

EXHIBIT 1

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