Qualcomm® Snapdragon™ 410E (APQ8016E) Windows Display
Overview
## Revision History

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>January 2018</td>
<td>Initial release</td>
</tr>
<tr>
<td>B</td>
<td>January 2018</td>
<td>Updated the document as per the branding changes</td>
</tr>
</tbody>
</table>
Section 1

Introduction
Objective

This document is intended for customers who are familiar with APQ8016E windows display, including:

- Distinction between display-related hardware and software components
- Display capabilities and performance benefits of the Multimedia Display Subsystem (MDSS)
- Control flow and data flow
- Basic information on source code layout, build, and debugging

Acronyms, abbreviations, and terms

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>ACPI</td>
<td>Advanced configuration and power interface</td>
</tr>
<tr>
<td>CABL</td>
<td>Content Adaptive Backlight Leveling</td>
</tr>
<tr>
<td>CAF</td>
<td>Content adaptive filter</td>
</tr>
<tr>
<td>CDD</td>
<td>Canonical Display Driver</td>
</tr>
<tr>
<td>DSPP</td>
<td>Destination surface processor</td>
</tr>
<tr>
<td>DSI</td>
<td>Display serial interface</td>
</tr>
<tr>
<td>GOP</td>
<td>Graphics Output Protocol</td>
</tr>
<tr>
<td>LM</td>
<td>Layer mix</td>
</tr>
<tr>
<td>MDSS</td>
<td>Multimedia Display Subsystem</td>
</tr>
<tr>
<td>SSPP</td>
<td>Source surface processor pipes</td>
</tr>
<tr>
<td>SBC</td>
<td>Smooth Backlight Control</td>
</tr>
<tr>
<td>WB</td>
<td>Write-back</td>
</tr>
</tbody>
</table>
Section 2

System Architecture
MDSS Overview

- Source surface processor (ViG, RGB, DMA – SSPP)
  - Format conversion and quality improvement for source surfaces (video, graphics, and so on)
- Layer mixer (LM)
  - Blend and mix source surface together
- Destination surface processor (DSPP)
  - Conversation, correction, and adjustment based on the panel characteristics
- Write-back/rotation (WB)
  - Write back to memory
  - Perform rotation if necessary
- Display interface
  - Timing generator and interface connection the display peripheral
Display Peripheral

- **MIPI DSI**
  - One MIPI DSI
  - Supports both smart and dumb displays
  - Up to four lanes support for each DSI
  - Up to 1.5 Gbps per lane with 24 bpp support
  - DATA±, CLK± (for one lane)
  - Supports up to 1280 × 800 resolution with 60 fps

- **WFD**
  - 1280 × 720 at 30 fps
The DSI controller is implemented to support the MIPI alliance standard for DSI.

The DSI controller includes one high-speed clock lane and one or more data lanes. Each lane is carried on two wires and uses low voltage differential signaling.

There are two modes of operations for DSI-compliant peripherals:

- Command mode
- Video mode
Feature Overview
Supported Interfaces

- APQ8016E supports up to two concurrent displays
  - DSI
    - Up to 1200 × 800 at 60 fps
  - Wi-Fi display
    - 1920 × 1080 at 60 fps

*Note:* The resolutions listed here are the maximum resolutions for an individual interface. When driving three displays simultaneously, it may be necessary to reduce the size of the connected displays. The end-to-end performance numbers might be different than the above.
## Source Surface Processor Pipes (SSPP)

<table>
<thead>
<tr>
<th>Feature</th>
<th>ViG</th>
<th>RGB</th>
<th>DMA</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of pipes</td>
<td>1</td>
<td>2</td>
<td>1</td>
</tr>
<tr>
<td>• 24-bit RGB (888)</td>
<td></td>
<td>• 24-bit RGB (888)</td>
<td>• 24-bit RGB (888)</td>
</tr>
<tr>
<td>• 16-bit RGB (565)</td>
<td></td>
<td>• 16-bit RGB (565)</td>
<td>• 16-bit RGB (565)</td>
</tr>
<tr>
<td>• 16-bit x/ARGB (4444,1555)</td>
<td></td>
<td>• 16-bit x/ARGB (4444,1555)</td>
<td>• 16-bit x/ARGB (4444,1555)</td>
</tr>
<tr>
<td>• 32-bit x/ARGB (8888) (with ARGB/RGBA/ABGR/RGBA and RGB/BGR premutation)</td>
<td></td>
<td>• 32-bit x/ARGB (8888) (with ARGB/RGBA/ABGR/RGBA and RGB/BGR premutation)</td>
<td>• YCbCr422 interleaved (YCrYCb, YCbYCr, CbYCrY, and CrYCbY)</td>
</tr>
<tr>
<td>• YCbCr422 interleaved (YCrYCb, YCbYCr, CbYCrY, and CrYCbY)</td>
<td></td>
<td></td>
<td>• AYCrCb444 interleaved</td>
</tr>
<tr>
<td>• AYCrCb444 interleaved</td>
<td></td>
<td></td>
<td>• YCbCr420 pseudo planar (NV12 and NV21)</td>
</tr>
<tr>
<td>• YCbCr420 pseudo planar (NV12 and NV21)</td>
<td></td>
<td></td>
<td>• YCbCr420 pseudo planar (NV12 and NV21)</td>
</tr>
<tr>
<td>• YCbCr422 pseudo planar (H1V2 and H2V1)</td>
<td></td>
<td></td>
<td>• YCbCr422 pseudo planar (H1V2 and H2V1)</td>
</tr>
<tr>
<td>• NV12/NV21 + alpha</td>
<td></td>
<td></td>
<td>• NV12/NV21 + alpha</td>
</tr>
<tr>
<td>• YCbCr422 pseudo planar + alpha</td>
<td></td>
<td></td>
<td>• YCbCr422 pseudo planar + alpha</td>
</tr>
<tr>
<td>• YCbCr420 planar</td>
<td></td>
<td></td>
<td>• YCbCr420 planar</td>
</tr>
<tr>
<td>• YCbCr422 planar</td>
<td></td>
<td></td>
<td>• YCbCr422 planar</td>
</tr>
<tr>
<td>Scaling ratio</td>
<td>Arbitrary 1/64-20x (decimation when &lt; 1/4)</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Sharpening</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Chroma up</td>
<td>Yes, any chroma sites</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>CSC</td>
<td>Yes</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td>Content adaptive contrast enhancement</td>
<td>• 256-bin histogram</td>
<td>No</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>• 256-entry LUT</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Flip</td>
<td>Vertical and horizontal flip</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>
### Layer Mixer, Background Color, and Hardware Cursor

<table>
<thead>
<tr>
<th>Feature</th>
<th>APQ8016E MDP support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of layer mixers</td>
<td>Two</td>
</tr>
<tr>
<td>Maximum number of surfaces blended</td>
<td>Four + hardware cursor + background color</td>
</tr>
<tr>
<td>Total number of pipes for blending</td>
<td>10 (1 ViG + 2 RGB + 1 DMA)</td>
</tr>
<tr>
<td>Alpha blending</td>
<td>Constant alpha, per pixel alpha, premultiplied alpha, modulation alpha – Reverse alpha for all the above</td>
</tr>
<tr>
<td>Alpha blending for background color</td>
<td>Yes</td>
</tr>
<tr>
<td>Background color generation</td>
<td>Yes (no data fetch for background color)</td>
</tr>
<tr>
<td>Transparency color key</td>
<td>Source color key, destination color key, simultaneous source and destination color key, and color key range</td>
</tr>
<tr>
<td>Arbitrary blending order</td>
<td>Yes</td>
</tr>
<tr>
<td>Blending in linear space</td>
<td>Yes</td>
</tr>
<tr>
<td>Blending color depth</td>
<td>12 bits/component</td>
</tr>
<tr>
<td>Hardware cursor size</td>
<td>128 x 128</td>
</tr>
</tbody>
</table>
## Destination Surface Processor Pipes (DSPP)

<table>
<thead>
<tr>
<th>Feature</th>
<th>APQ8016E MDP support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sunlight visibility improvement (SVI)</td>
<td>Yes</td>
</tr>
<tr>
<td>CABL</td>
<td>Yes</td>
</tr>
<tr>
<td>Panel color correction (PCC)</td>
<td>$3 \times 11$ polynomial</td>
</tr>
<tr>
<td>Bit-depth for color correction</td>
<td>12 bits/component</td>
</tr>
<tr>
<td>Gamma correction</td>
<td>Yes (Three-channel LUT)</td>
</tr>
<tr>
<td>Picture adjustment (hue, saturation, contrast, and intensity)</td>
<td>In HSV space, smooth curve soft clip</td>
</tr>
<tr>
<td>Dither</td>
<td>$4 \times 4$ ordered dithering performed without panel depth reduction</td>
</tr>
<tr>
<td>Memory color (sky, foliage, and skin tone)</td>
<td>Yes</td>
</tr>
<tr>
<td>Six-color zone adjustment</td>
<td>Yes</td>
</tr>
</tbody>
</table>
## Rotator and WB

<table>
<thead>
<tr>
<th>Feature</th>
<th>APQ8016E MDP support</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Rotator</strong></td>
<td></td>
</tr>
<tr>
<td>Input format support</td>
<td>Same as ViG</td>
</tr>
<tr>
<td>Rotation modes</td>
<td>90°, 180°, and 270°</td>
</tr>
<tr>
<td><strong>WB</strong></td>
<td></td>
</tr>
<tr>
<td>Number of WBs</td>
<td>Two, WB0 and WB2</td>
</tr>
<tr>
<td>WB performance</td>
<td>WB0 – 1280 × 800 @ 60 fps and WB2 – 1280 × 720 @ 30 fps</td>
</tr>
<tr>
<td>WB format</td>
<td>• 24-bit RGB (888)</td>
</tr>
<tr>
<td></td>
<td>• 16-bit RGB (565)</td>
</tr>
<tr>
<td></td>
<td>• 16-bit x/ARGB (4444, 1555)</td>
</tr>
<tr>
<td></td>
<td>• 32-bit x/ARGB (8888) – With ARGB/RGBA/ABGR/RGBA and RGB/BGR permutation</td>
</tr>
<tr>
<td></td>
<td>• YCbCr420 pseudo planar (NV12, NV21)</td>
</tr>
<tr>
<td></td>
<td>• YCbCr422 pseudo planar (H1V2, H2V1)</td>
</tr>
<tr>
<td></td>
<td>• NV12</td>
</tr>
<tr>
<td></td>
<td>• YCbCr422 pseudo planar</td>
</tr>
<tr>
<td></td>
<td>• YCbCr420 planar</td>
</tr>
<tr>
<td></td>
<td>• YCbCr422 planar</td>
</tr>
</tbody>
</table>
# Wireless Display

<table>
<thead>
<tr>
<th>Feature</th>
<th>APQ8016E MDP support</th>
</tr>
</thead>
<tbody>
<tr>
<td>Number of WBs</td>
<td>One, WB2 with display processing</td>
</tr>
<tr>
<td>WB performance</td>
<td>WB2 – 720p at 30 fps</td>
</tr>
<tr>
<td>WB format</td>
<td>• 24 bit RGB (888)</td>
</tr>
<tr>
<td></td>
<td>• 16 bit RGB (565)</td>
</tr>
<tr>
<td></td>
<td>• 32bit x/ARGB or BGRx/A (8888)</td>
</tr>
<tr>
<td></td>
<td>• YCbCr420 pseudo planar (NV12)</td>
</tr>
<tr>
<td>Composition</td>
<td>WB for the final composition surface and WB2 with hardware cursor</td>
</tr>
</tbody>
</table>
Section 4

Display and Video Processing Features
### Scaling

<table>
<thead>
<tr>
<th>Feature</th>
<th>ViG pipe</th>
<th>RGB pipe</th>
</tr>
</thead>
<tbody>
<tr>
<td><strong>Scaling</strong></td>
<td></td>
<td>No</td>
</tr>
<tr>
<td>Scaling ratio</td>
<td>1/64-20x (decimation for &lt;1/4)</td>
<td></td>
</tr>
<tr>
<td>Upscaling filter</td>
<td>• 4-tap CAF (32 phases)</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>• 2-tap bilinear (32 phases)</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Nearest neighbor (32 phases)</td>
<td></td>
</tr>
<tr>
<td>Downscaling filter</td>
<td>PCMN (8-phase)</td>
<td>No</td>
</tr>
<tr>
<td>Chroma up</td>
<td>• 420→444 and 422→444</td>
<td>No</td>
</tr>
<tr>
<td></td>
<td>• Combined with scaler</td>
<td></td>
</tr>
<tr>
<td></td>
<td>• Any chroma sites by programming initial phase</td>
<td></td>
</tr>
</tbody>
</table>

*CAF – Content adaptive filter; adjust filter coefficients based on content
*PCMN – Phase control M/N; fractional averaging filter for downscaling; fractional is done with the 8-phase PCMN, for example, uses 3.375 (27/8) averaging filter for 3.375:1 downscaling

2x by 4 × 2  
2x by QSEED2  
48/100 AVG  
48/100 QSEED2
## Sharpening

<table>
<thead>
<tr>
<th>Feature</th>
<th>ViG pipe</th>
<th>RGB pipe</th>
</tr>
</thead>
<tbody>
<tr>
<td>Sharpening/smoothing</td>
<td>• -256 to 255 – Negative means smoothing and positive means sharpening</td>
<td>N/A</td>
</tr>
<tr>
<td></td>
<td>• Combined with scaling filter</td>
<td></td>
</tr>
</tbody>
</table>

*Before* and *After* images show the effect of sharpening on the image.
Noise Injection/Dithering

- Reduces banding artifacts by adding random noise
- Two types of banding artifacts, two types of dithering
  - Destination dithering – Reduces banding artifacts due to insufficient color depth of the panel; for example, 24 bpp content on 18 bpp panel
  - Source dithering – Reduces banding artifacts in content even though both content and panel are true colors
Adaptive Backlight – Global CABL

<table>
<thead>
<tr>
<th>Feature</th>
<th>APQ8016E MDSS</th>
</tr>
</thead>
<tbody>
<tr>
<td>Process space</td>
<td>V (maximum (R,G,B)) of the HSV space</td>
</tr>
<tr>
<td>Histogram collection</td>
<td>Hardware, 256 bins</td>
</tr>
<tr>
<td>LUT</td>
<td>Hardware, 256 bins</td>
</tr>
<tr>
<td>Pipeline location</td>
<td>After blending and picture adjustment</td>
</tr>
<tr>
<td>Core algorithm</td>
<td>Software</td>
</tr>
</tbody>
</table>

- Better visual quality with separated LUT for gamma correction and ABL
- Compensates impact of panel characteristic change due to backlight level variation
- Backlight savings of up to 55% possible but depends on the final OEM configuration
Sunlight Visibility Improvement (SVI)

SVI is a Qualcomm® Technologies, Inc. (QTI) proprietary global tone adjustment solution to improve the display visibility in bright, ambient light environments without boosting panel backlight/brightness.

**Figure:** Camera shot taken on commercial device under different ambient lights, from left to right, with ambient light value 500 lux, 1000 lux, 2000 lux, 5000 lux, and 10000 lux.
Actual Example

Extremely strong ambient light (33,400 lux)

without SVI, 100% BL

with SVI, 100% BL
Section 5

Picture Adjustment
Picture Adjustment (HSIC)

Hue

Saturation

Brightness
Windows on Snapdragon (WoS)
Unified Extensible Firmware Interface (UEFI)
Platform boot consists of three stages:

- SBL boot loaders, UEFI, and the main operating system.
- The first two stages are non persistent; execution code is lost at the next stage.
- The only persistent code between UEFI and the operating system is Advanced configuration and power interface (ACPI).

Windows has two display driver modes:

- Canonical Display Driver (CDD)
  - Used during bootup, but also used when the miniport is not loaded or upgraded.
- Display/graphics miniport driver
  - Provides accelerated display, graphics, and video functionality.
**Display – UEFI**

- **UEFI**
  - Replacement for BIOS in the desktop world or customized boot loaders in the mobile world.
  - The QTI reference version of UEFI is based on EDK2 (EFI's open source implementation of UEFI).
  - QTI reference platform UEFI is recommended for licensee use.
  - A full source for QTI reference platforms is available to licensees.

- **Display falls under the Display Dxe module category**
  - All display code falls under a single Dxe module with dependencies on other system modules such as PMIC, GPIO, and clocks
  - QTI’s reference platforms implement the standard graphics output protocol (EFI_GRAPHICS_OUTPUT_PROTOCOL)
Graphics Output Protocol (GOP)

- Standard EFI protocol
  - EFI_GRAPHICS_OUTPUT_PROTOCOL_QUERY_MODE
    - QueryMode – Used to query the set of available display modes
  - EFI_GRAPHICS_OUTPUT_PROTOCOL_SET_MODE
    - SetMode – Used to set the display to a specific mode
  - EFI_GRAPHICS_OUTPUT_PROTOCOL_BLT
    - Blt – Used to bit application data to the screen
  - EFI_GRAPHICS_OUTPUT_PROTOCOL_MODE
    - Mode – Pointer to the current mode information
UEFI Driver Structure
Section 7

WoS ACPI
ACPI

- Open standard for device configuration – Windows relies heavily on ACPI to enumerate device driver, and provides configuration and resource information for all Windows drivers.
- Full source to ACPI tables are provided to licensees.
- QTI reference supplies sample ACPI configuration to install and enumerate all resources for display, graphics, and video encoder/decoders.
- ACPI also defines extension methods to allow licensees to customize their platforms.
  - None of the extensions are mandatory in Windows 8; it is up to the discretion of the miniport driver writer to use these extensions.
  - QTI provides samples for a few select display extensions. Most of the extensions are not supported by the QTI driver; however, licensees are free to implement and call ACPI methods in their own drivers.
  - Writing ACPI methods is even more limited than UEFI drivers; supporting complex drivers like DSI or HDMI in ACPI is impossible.
The bitmap is displayed on screen by UEFI.

A static BGRT table is used to communicate BMP information to the operating system.
ACPI Structure

ACPI – Power management

Graphics_resources.as
- Components
- F States
- P States

ACPI – Resources and configuration tables

dsdt.asl
- MMIO
- GPIO
- I²C

graphics.asl

display.asl
- _ROM
- PIGC
- PPCC
- PGCT
- PGRT
- PBRT

panelcfg.asl

backlight.asl
-BLCP

Sec. 7
Section 8

WoS WDDM Model
WDDM Model

- Graphics kernel mode driver
  - Graphics driver and scheduler; direct interface to the Dxgkrnl DDI interface
- Display export driver
  - Display driver based on QDI interface; a separate driver is installed along with graphics KMD
- User mode components
  - D3D UMD
    - Manages all 3D rendering commands going to the GPU
  - D3D Video UMD
    - Manages all video commands to the video core and MDP bit engine
- Kernel mode components
  - Graphics KMD (also known as miniport)
    - Manages scheduling, surface allocation, GPU power management, source/target path, overlays, and hardware IP communication
    - Abstracts PEP/MSFT interfaces from QDI/Video engines and communication with other drivers
  - Display KMD
    - Hardware control of primary display, HDMI, overlays, bit operation, and rotation
  - Video KMD
QDI Driver Model

Miniport
('displayLib', 'display', 'nbpbblib', 'rotatorLib')

QDI Export ('main')
QDI ('main')

PAL Library ('pal')

OSAL Library ('osal')

PMIC Driver

MSFT WDK

DSI Driver ('paneldriver')
edP Driver ('paneldriver')
HDMI Driver ('paneldriver')

DSI Host ('DSIHost')
edP Host ('eDPHost')
HDMI Host ('HDMIHost')

HAL ('hal\mdp')

DSI HAL ('hal\dsi')
edP HAL ('hal\edp')
HDMI HAL ('hal\hdi')

MDP Registers

QDI Display Driver

DSI Registers (Controller, Phy, PLL)
edP Registers (Controller, Phy, PLL)
HDMI Registers (Controller, Phy, PLL)
QDI Driver Modules

- QDI export
  - Special interface to the miniport
  - Interrupt handlers, DPC handlers, driver resource (MMIO, GPIO, and I²C resources) registration.
- QDI
  - Standard QDI2 interface
  - Device, display, layer context handles, and management.
- PAL library
  - Platform abstraction layer
  - Miniport specific callbacks for ACPI manipulation, power management, GPIO, I²C resource handling, and communication with PMIC (WLED and LPG)
- OSAL library
  - Operating system services abstraction, mutex, threads, delays, C Library (memcpy, memset), logs, and memory allocation.
- DS
  - Display services layer, display resource management, display, device, and layer control
  - Rotator, bit management
  - SMP management
- Panel drivers
  - Handle call sequencing and into eDP, DSI, and HDMI drivers
- Host drivers
  - Interface management of eDP, HDMI, and DSI protocols
Section 9

Windows Display Driver
Display Engine Concept

- Dxgkrl manages display, graphics, and video kernel mode components as engines.
- Each engine is power managed separately and can be reset when it is nonresponsive (TDR).
- A TDR (timeout detection and recovery) is a method for windows to reset an engine if it does not respond to a command within an allowed timeout.
  - Display engine TDR – Occurs when the presented surface is not reported back during a Vsync interrupt due to following reasons:
    - Caused by lack of Vsync interrupt
    - Vsync interrupt took too long to occur
    - Surface (or surfaces) reported during a Vsync does not match the presented surface
  - Rotator/Bit TDR – Occurs when an operation fails to report a completion interrupt.
    - Hardware not reporting a complete interrupt as it goes into a loop or operation did not occur
WoS Platform Customization
Display customization for QTI reference platforms is performed entirely through the panel configuration file.

- A human readable file (.xml-like) contains all the necessary fields and configuration to describe any active or smart panel.

- Panel configuration is split into several sections:
  - EDID configuration – Windows requires a valid EDID to be presented for all internal and external panels; the panel .xml file requires manufacture ID, product ID, and other EDID-specific fields. Other fields (detailed timings) are simplified and retrieved from timing fields.
  - Timing fields – Active timing information, including active sizes, front/back porches, and pixel clock configuration.
  - Command fields – For DSI panels that support commands, the panel configuration file allows the licensee to send commands for specific events, such as panel initialization and panel shutdown.
  - Backlight control – Panels that require support backlight adjustment through PMIC or DSI commands are configured through the panel driver.
Panel configuration file customization

- For UEFI, the panel driver is included in the UEFI code at compile time.
  - edk2\QcomPkg\Msm8974Pkg\Library\MDPPlatformLib\MDPPlatformLib.c
- For the miniport, the panel driver is compiled into the ACPI tables via the _ROM method, which is a standard method to supply the miniport with proprietary information.
  - panelcfg.asl, backlightcfg.asl, display.asl, and pep.asl
- Although QTI reference platforms only use a panel configuration file, it is expected that OEMs require **extra** controls to **fine-tune** their platforms.
  - UEFI – Full UEFI source is available to OEMs; any customizations are done directly at a source level within UEFI.
  - Miniport – An OEM owned panel driver can be created to directly interface to the miniport driver.
QTI provides a skeleton OEM panel driver

- A published interface is defined to allow OEMs to override or customize a subset of miniport functions.
  - Oem_qdi.h (in QCDK)
  - OEM panel driver interface specification

- OEMs own their respective panel drivers and do not need to publish this back to QTI. OEMs are required to supply a binary version of the OEM driver to debug platform-specific issues that cannot be reproduced without the OEM driver.

- OEMs must abide by the OEM panel driver interface including rules for reentrancy, IRQL, and memory types (paged vs. nonpaged buffers).

- OEMs are responsible for installing their own panel driver, including any ACPI entries to facilitate driver installation.

- Calling other drivers from the panel driver may require parent/child decencies or PnP notifications to be handled.

- OEMs do not directly control the power states of the MDP hardware and interface cores. All power and performance controls are done through PEP ACPI entries (pep.asl).
Section 11

Gamma and Color Correction on WoS
Display Color Calibration

- Panels inherently have different behaviors between manufactures, models, and even between individual panels.
- Involves four components:
  1. Modify panel gamma LUT to correct **panel tone**.
     - Based on the panel LUT table gathered from display calibration to define matching gamma curve (MGC).
  2. Modify display CSC block to correct **panel color**.
     - Modify 3×3/3×11 matrix to adjust panel response based on data from display calibration.
  3. Modify gamma LUT to correct **picture gamma**.
     - Apply gamma correction on a picture based on a set of predefined gamma curves (REC601, REC709, and so on)
  4. Modify display CSC block to **dynamically adjust** hue, saturation, and intensity of the content.
     - Adjust 3×3/3×11 matrix to manipulate hue, saturation, and intensity based on application control.
     - Same feature can be applied at the display pipe as well as VG layer pipes.
ACPI Entries for Panel Calibration

- The panel calibration data is stored in the ACPI table, and the data is read out during the panel initialization, and then get programmed into hardware blocks.
- There are three ACPI methods defined for driver to retrieve the corresponding data:
  - PIGC – To retrieve panel inverse gamma correction data (3 × 256 256 × 16 bits)
  - PPCC – To retrieve panel color correction data (3 × 11 11 × 64 bits)
  - PPGC – To retrieve panel gamma correction data (3 × 16 16 × 32 bits)
Color Management Blocks

- PIGC
  - Inverse gamma table
- PGRT
  - Gamma response table
- PPCC
  - Polynomial color correction table
- PGCT
  - Gamma correction table
- PBRT
  - Backlight response table
Panels may not have a linear response to the backlight level applied to them.
Entry measurement is on PBRT to linearize the curve.
Backlight Response Mapping Overview

- Backlight response mapping serves as a calibration of backlight response so that correct luminance is achieved.
- The OEM calibrates panels and stores the response table in ACPI.
- Calibration involves an accurate measurement of luminance.
- A display driver uses this table to do the mapping as the last stage of backlight calculations.
Section 12

Backlight and Image Optimizations
Smooth Backlight Control (SBC)

- SBC is a feature to make backlight changes smooth instead of drastic or instantaneous.
- Applies to all backlight changes made by the user or the operating system, except when turning off backlight (needs to be immediate).
Content Adaptive Backlight Leveling (CABL)

System-wide processing of backlight (except assertive display)
Algorithm to reduce power by analyzing the frame contents.

- **Backlit (LCD) displays**
  - Algorithm reduces backlight level
  - Algorithm compensates by boosting pixel values using a LUT
  - Algorithm pursues maintaining image fidelity, but it could be degraded

- **AMOLED displays**
  - Displays without backlight, each pixel emits its own light
  - Algorithm reduces pixel values
  - Algorithm enhances contrast
  - Image fidelity loss is unavoidable (may not be perceptible)
Windows operating system controls dynamically the following parameters:

- CABL enable/disable
  - Enabled when using battery power
  - Disabled when plugging a power adapter

- CABL power savings setting based on use case
  - UI/Desktop – low-power savings
  - Full screen video – high-power savings
  - Dimmed – medium power savings
Section 13

MDP Extensions in Qualcomm® Adreno™ OEM Debugger Extension
### MDP Extensions in Adreno OEM Debugger Extension

<table>
<thead>
<tr>
<th>Command</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>!mdp_chipid</td>
<td>Displays the MDP chip ID</td>
</tr>
<tr>
<td>!mdp_int_status</td>
<td>Returns MDP enabled interrupts and status with an option to clear</td>
</tr>
<tr>
<td>!mdp_mixer_info</td>
<td>Returns the MDP layer/mixer routing and hardware status</td>
</tr>
<tr>
<td>!mdp_layer_info</td>
<td>Returns the MDP layer configuration information</td>
</tr>
<tr>
<td>!mdp_axi_info</td>
<td>Returns the MDP AXI routing and status</td>
</tr>
<tr>
<td>!mdp_blend_info</td>
<td>Returns the MDP blending configuration</td>
</tr>
<tr>
<td>!mdp_cursor_info</td>
<td>Returns the MDP cursor configuration</td>
</tr>
<tr>
<td>!mdp_status</td>
<td>Returns the MDP hardware status</td>
</tr>
<tr>
<td>!mdp_bist</td>
<td>Enables/disables the MDP built-in-self test</td>
</tr>
<tr>
<td>!mdp_reg_base</td>
<td>Configures the base address for mdp_rr and mdp_wr</td>
</tr>
<tr>
<td>!mdp_rr</td>
<td>Read the MDP register at offset</td>
</tr>
<tr>
<td>!mdp_wr</td>
<td>Write the MDP register at offset with value</td>
</tr>
<tr>
<td>!mdp_dump_regs</td>
<td>Dump all the MDP registers to file</td>
</tr>
<tr>
<td>!mdp_screencapture</td>
<td>Perform a MMU-based screenshot of the frame buffer</td>
</tr>
</tbody>
</table>
Questions?

For additional information or to submit technical questions, go to:
https://discuss.96boards.org/c/products/dragonboard410c
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