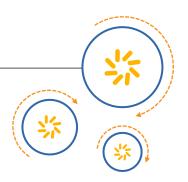


Qualcomm Technologies, Inc.



## **RB04**

### Hardware Reference Guide

80-YA116-25 Rev. A

October 31, 2017

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## **Revision history**

Revision	Date	Description	
A	October 2017	Initial release	

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# 1 Introduction

The RB04 board brings out interfaces supported by QCA4010 in minimal PCB form factor. The RB04 interfaces can be easily and safely accessed via RB01. The functional mode of the RB04 board is decided by the bootstrap configuration on RB01, which meanwhile facilitates evaluation of QCA4010 power consumption and Wi-Fi performance.

The combination of RB04 and RB01 forming an evaluation platform can also be used for software development of QCA4010-based systems.

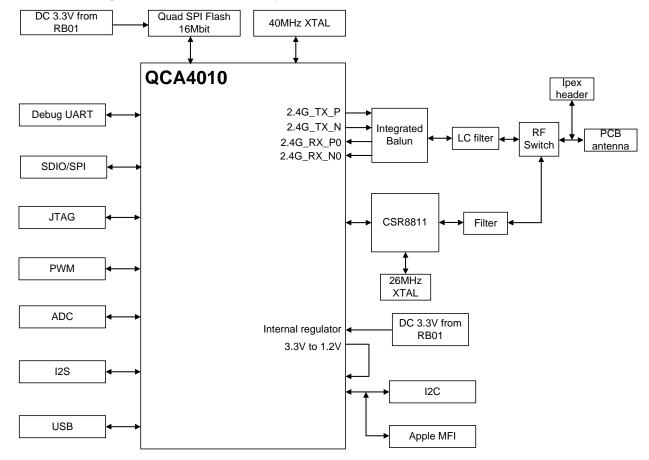


Figure 1-1 RB04 block diagram

# 2 RB04 component and interface

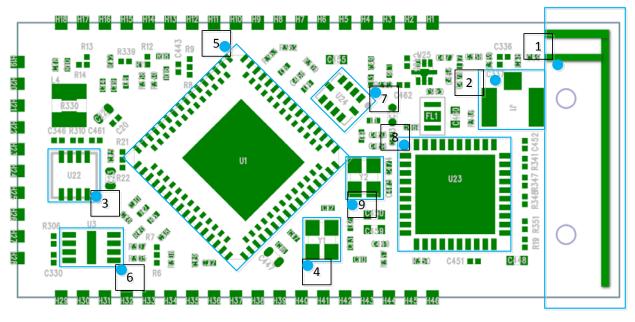


Figure 2-1 RB04 reference design module (front view)

NOTE: The picture is for reference only.

#### Table 2-1 RB04 details

1	2.4 GHz Printed Antenna		
2	Tx/Rx RF Ipex Conn		
3	Apple MFI		
4	40 MHz Crystal		
5	QCA4010 Area		
6	16 Mbit Quad SPI Flash		
7	Integrated Balun		
8	CSR8811 Area		
9	26 MHz Crystal		

## 2.1 RB04 main components

Table 2-2 lists the components contained in RB04.

#### Table 2-2 Components list

Component	Description		
2.4 GHz Printed Antenna	Printed Inverted F Antenna for 2.4 GHz Band		
TX/RX RF Ipex Connector	RF Connector for Transmitting and Receiving RF signal measurement		
Apple MFI	Apple certification IC		
40 MHz Crystal	Provide 40 MHz Reference Clock for Wi-Fi		
26 MHz Crystal	Provide 26 MHz Reference Clock for BT		
QCA4010	Refer to QCA4010 Device Specification		
CSR8811	Refer to CSR8811 Datasheet		
SPI Flash	The 16 Mbit SPI flash supports quad mode		
Integrated Balun	Single Balun IC to minimize cost, size, tuning and tolerance		

#### 2.2 RB04 RF section

The RF section contains 2.4 GHz RF Balun, Band-trap Filter, RF Matching Circuit.

#### 2.3 RB04 interface

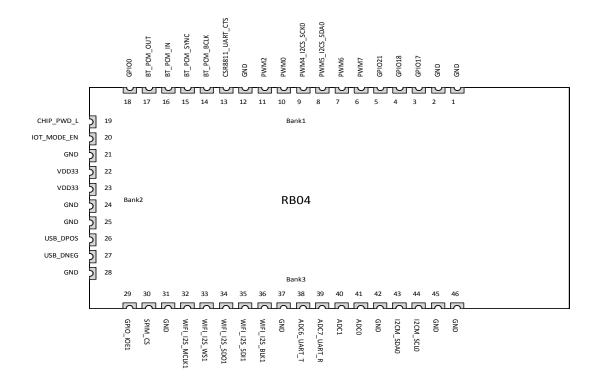
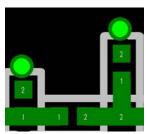


Figure 2-2 RB04 module interface definition (top view)

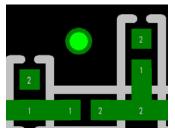
### 3.1 GND

#### 3.1.1 Placement of capacitor shunted to GND

- Place bypass capacitors as close to the respective pins as possible.
- Place at least one dedicated ground via for each capacitor shunted to ground and put ground via as close to the capacitors as possible:



Good capacitor placement (2 capacitors with 2 dedicated ground vias)



Bad capacitor placement (2 capacitors sharing only 1 ground via)

#### 3.1.2 GND

Avoid large ground planes without ground vias. The ground plane shown in Figure 3-1 can act like an antenna radiating unwanted signals to other parts of the reference board.

9



Figure 3-1 Example: ground plane without ground vias

#### 3.1.3 SDIO

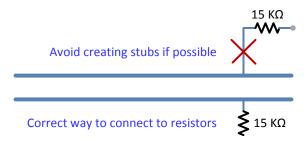
- Use ground trace for SDIO routing to isolate SD\_CLK.
- Avoid routing parallel to SD\_CLK (above, underneath and on both sides); SD\_CLK can run up to 50 MHz and can couple to other traces.
- Keep the reference ground plane of SDIO lines as solid as possible.
- Route SDIO lines on inner layers to avoid picking up noise.

Gr	ou	nd	

SD_CMD	🗘 10 mil
SD_D3	
SD_D2	
SD_D1	
SD_D0	
	🗘 10 mil
SD_CLK	🗘 10 mil
	10 mil

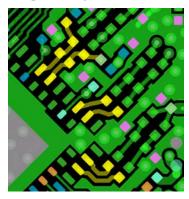
#### 3.2 USB

- Use 90  $\Omega$  differential lines to rout USB D+/D-.
- Avoid routing USB lines close to the edge of the board.
- Avoid routing USB lines with 90° turns. Use 45° transition.
- Avoid placing stub components on the USB data lines.



### 3.3 RF Routing

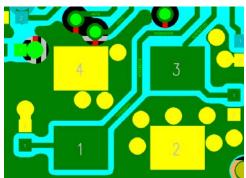
- Route all differential and single-ended traces for RF signal with an impedance of 50 Ω. Avoid right angle line routing.
- Keep the length of the RF differential output traces as short as possible.



• Use separate vias to tie all the power pins to the power traces or power plane. Do not make the power pins share the same VDD via.



- Avoid power trace routing underneath the QCA4010.
- Enclose the crystal traces with ground plane and avoid routing power traces underneath the crystal.



If power planes are used, avoid via holes as they will break the integrity of the power plane.
Figure 3-2 shows how via holes can block the current path on the power plane.

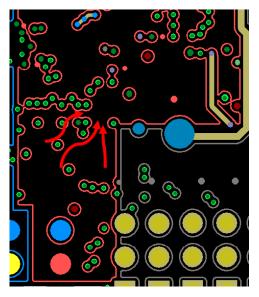


Figure 3-2 Example: via holes blocking the current path on the power plan

#### 3.4 Board stack-up

The RB04 reference design is implemented on a four-layer board:

- Layer 1 is for RF and signal traces.
- Layer 2 is the ground plan.
- Layer 3 is for power and signal.
- Layer 4 is for signal and ground.

The RB04 consists of the elements listed in this section with the board stack-up as shown in Table 3-1.

- 4-layer board
- Total stack thickness: 39.8 mil/1 mm
- Material: FR4 Tg 140
- Dielectric constant 4.25 @ 5 GHz

#### Table 3-1 RB04 reference design board stack-up

4 layer stack-up for 1 mm +/- 0.15mm board thickness		Thickness (mil)	Thickness (mm)		
			Solder mask	0.7	0.018
L1			Copper foil 0.333oz + Plating	1.2	0.03
FR4			Core 2.8mil	2.8	0.071
L2			Copper foil 0.5oz	0.65	0.0165
FR4		PTH	Core 28mil	28	0.711
L3		1-4	Copper foil 0.5oz	0.65	0.0165
FR4			Core 2.8mil	2.8	0.071
L4			Copper foil 0.333oz + Plating	1.2	0.03
			Solder mask	0.7	0.018
	Total		38.7	0.982	