## Revision history

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<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>A</td>
<td>July 2017</td>
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</tr>
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1 Introduction

NOTE: This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software. Enabling some features may require additional licensing fees.

An Input/Output Buffer Information Specification (IBIS) file contains the data required to model the input, output, and input/output buffers of a component. The data in an IBIS file helps to build a buffer model used in signal integrity (SI) simulations of high-speed boards and systems. This document provides the overview of IBIS models released by Qualcomm Technologies, Inc (QTI).

Designers often simulate their printed circuit boards (PCBs) before they have devices to test. The IBIS models allow designers to simulate the I/O behavior and analyze the various components on their board using the IBIS files.

1.1 Scope

Hardware design engineers and developers responsible for performing the time measurements and SI tests can refer to this document for information that is required to enable an accurate design, using a simulation.

IBIS models are generated from the Simulation Program with Integrated Circuit Emphasis (SPICE) simulations and are compared with the silicon data to model the real device as closely as possible.

This document gives guidance when selecting the correct IBIS model to simulate and analyze the I/O device.

1.2 References

For more details related to IBIS, see the following links:

- IBIS specifications: https://ibis.org/specs/
- IBIS modeling cookbook: https://ibis.org/cookbook/
2 Overview of IBIS models

IBIS is a standard for describing the analog behavior of the buffers of digital devices using plain American Standard Code for Information Interchange (ASCII) text formatted data. IBIS files are not models, but they contain the data required to model the input, output, and I/O buffers of a component.

The advantages of IBIS over SPICE are the following:

- It has faster simulation time.
- It does not contain any confidential circuit design or process information.

This buffer model describes the I/O characteristics of a device through current/voltage (I/V) and voltage/time (V/T) data.

For example, an IBIS file of a device contains the electrical characteristics of all the unique pins of that device.

The IBIS format provides the minimum, typical, and maximum corner data within each individual model.

The IBIS file also contains the package resistance, inductance, and capacitance (R, L, and C) data for each pin.

The following are the three types of IBIS models:

- Input
- Output
- I/O

Input

An input model functions as a receiver. The input pin structure of a digital device is a combination of the following circuits and elements:

- A circuit that is activated if the input voltage is over $V_{DD}$ or logic high (power clamp)
- A circuit that is activated if the input voltage is below ground or logic low (ground clamp)
- A circuit that is activated if the input is within $V_{DD}$ and ground (active circuit)
- Resistance, inductance, and capacitance of the package (R, L, and C respectively)

Figure 1 shows the input model of an IBIS file.
Output

An output model functions as a driver. The output pin is a combination of the following elements and circuits:

- A pull-up circuit that is activated when the output voltage is high
- A pull-down circuit that is activated when the output voltage is low
- Die capacitance of the output pin
- R, L, and C of the package

Figure 2 shows the output model of an IBIS file.
Input/Output (I/O)

In the I/O model, the pin is connected to device cells, and it can function either as a driver or a receiver based on the enabling logic.

NOTE: This model sources and/or sinks current and thus cannot be disabled.
Figure 3 shows the I/O model of an IBIS file.

2.1 Create an IBIS model

IBIS files are created by simulation or from bench measurements.

To generate an IBIS model, use these steps:

1. Perform the following premodeling steps:
   a. Obtain the packaging information.
   b. Determine the voltage and temperature tolerances over which the integrated circuit (IC) is specified to operate.

2. Obtain the details related to the following:
   a. I/V curves.
   b. Rise/fall times for output or I/O buffers.

This data is obtained either by direct measurement or by simulation.
2.2 Overview of IBIS file

QTI uses internal tools to generate IBIS models with the following versions:

- IBIS 4.2: Used for signal integrity analysis
- IBIS 5.0: Used for power aware signal integrity analysis
- IBIS Algorithmic Modeling Information (AMI) models: These are special models intended for signal integrity of high-speed SerDes. These algorithmic models allow simulation with various SerDes features such as equalizer, pre-emphasis, de-emphasis, jitter parameter, and so on.

The following are the major sections of an IBIS file:

- The header provides the details related to the IBIS version, file name, and file revision.
- Component details contain the pin information of the device, which includes pin lists, package information, and pin-to-buffer mapping.
- V-I behavioral models contain the data that is required to recreate I-V curves and V-t transition waveforms, which describe the switching properties of a particular buffer.
- Model selector contains the details related to the various simulation models available for a particular buffer. Model selector is used to select different I/O operating modes.

Some of the options available in model selectors include the following:

- Drive strength
- Slew rate
- Voltage mode

2.2.1 Measurement conditions of IBIS models

IBIS models are generated for the following corner conditions:

- Typical
  - Nominal voltage supply
  - Nominal temperature
  - Nominal process parameters
- Minimum
  - Lowest voltage supply
  - High temperature
  - Weak process parameters
- Maximum
  - Highest voltage supply
  - Low temperature
  - Strong process parameters
2.2.2 View an IBIS file

IBIS files are plain text files that can be opened in any text editor. However, for a better reading experience, they can be opened in the visual IBIS Editor. Various free tools including Visual IBIS editors can be downloaded from https://ibis.org/tools/.

2.3 IBIS naming convention

This section provides basic information about the naming convention used for different models in IBIS. While understanding the naming convention is not required to perform signal integrity, it provides brief understanding to PCB and hardware designer about the various features of an IBIS model.

The name of and IBIS model includes following basic information:

- type of the I/O driver/receiver
- drive strength of the model
- voltage used

IBIS models can work on multiple voltages and drive strengths. The maximum number of characters for an IBIS model name is 18.

Some of the examples for IBIS naming convention include the following:

Example 1

Type_<initial drive to final drive strength (in mA)>_<operating voltage >_<type> OR
Type_<initial drive to final drive strength (in mA)>_<type>_<operating voltage >

Type defines the pin type.

Table 1  IBIS naming – sample 1

<table>
<thead>
<tr>
<th>Format</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c_216_26</td>
<td>A complementary metal oxide semiconductor (CMOS) type pin with a drive strength between 2 mA and 16 mA and an operating voltage of 2.6 V</td>
</tr>
<tr>
<td>s_216_26_nb</td>
<td>A Schmitt nobscan type pin with a drive strength between 2 mA and 16 mA and an operating voltage of 2.6 V</td>
</tr>
<tr>
<td>s_28_26_hv</td>
<td>A Schmitt high voltage type pin with a drive strength between 2 mA and 8 mA and an operating voltage of 2.6 V</td>
</tr>
<tr>
<td>s_216_nl_18</td>
<td>A Schmitt no latch type pin with a drive strength between 2 mA and 16 mA and an operating voltage of 1.8 V</td>
</tr>
<tr>
<td>s_216_nbnl_18</td>
<td>A Schmitt no latch and no boundary scan type pin with a drive strength between 2 mA and 16 mA and an operating voltage of 1.8 V</td>
</tr>
</tbody>
</table>

Example 2

Type_<initial drive to final drive strength (in mA) or total drive options>_<operating voltage>_<type>_<simulated voltage>_<settings>

Type defines the pin type and simulated voltage defines the voltage at which the buffer is simulated for specific drive settings.

**NOTE:** The simulated voltage can be less than or equal to the voltage for normal operation.
Table 2  IBIS naming – sample 2

<table>
<thead>
<tr>
<th>Format</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>s_216_26_18_010</td>
<td>A Schmitt type pin with a drive strength between 2 mA and 16 mA and an operating voltage of 2.6 V; the buffer is simulated at 1.8 V with the drive setting as 010.</td>
</tr>
<tr>
<td>s_47_18_110</td>
<td>A Schmitt type pin with a drive strength between 4 mA and 7 mA and an operating voltage of 1.8 V; the buffer is simulated at 1.8 V with the drive setting as 110.</td>
</tr>
<tr>
<td>s_216_26_nla_26_001</td>
<td>A Schmitt_nolatch type pin with a drive strength between 2 mA and 16 mA and an operating voltage of 2.6 V; the buffer is simulated at 2.6 V with the drive setting as 001.</td>
</tr>
<tr>
<td>s_8drv_srtctl_00_18_011</td>
<td>A Schmitt_slewratecontrol type pin with eight drive strength options and an operating voltage of 1.8 V; the buffer is simulated at 1.8 V with the drive setting as 011 and the slew rate setting as 00.</td>
</tr>
<tr>
<td>s_216_nolvlshft_18_000</td>
<td>A Schmitt_nolevelshift type pin with a drive strength between 2 mA and 16 mA drive strength options and an operating voltage of 1.8 V; the buffer is simulated at 1.8 V with the drive setting as 000 and the slew rate setting as 00.</td>
</tr>
</tbody>
</table>

Example 3

<Type with interface details>_<simulated voltage>_<settings>

Type defines the pin type. For special interfaces like USB, SGMII, and LPDDR2, the Type is described with interface name and pin details. simulated voltage defines the voltage at which the buffer is simulated for specific settings. Settings can be drive strength and/or slew rate. In some cases, additional settings are also allowed. Details of these additional settings can be found in the Model Selector section of the buffer in IBIS file.

NOTE: The simulated voltage can be less than or equal to the voltage for a normal operation.

Table 3  IBIS naming – sample 3

<table>
<thead>
<tr>
<th>Format</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>lpddr2_dq_12_10011</td>
<td>A LPDDR2 DQ pin with an operating voltage of 1.2 V; the buffer is simulated at 1.2 V with the drive setting as 100 and the slew rate setting as 11.</td>
</tr>
<tr>
<td>hsic_dq_12_01000</td>
<td>A HSIC DQ pin with an operating voltage of 1.2 V; here the buffer is simulated at 1.2 V with the drive setting as 010 and the slew rate setting as 11.</td>
</tr>
<tr>
<td>qmp_sgmii_tx_1225_00000</td>
<td>A SGMII TX pin with an operating voltage of 1.225 V; here the buffer is simulated at 1.225 V with the drive setting as 00000.</td>
</tr>
<tr>
<td>tcxo_18</td>
<td>A TCXO pin with an operating voltage of 1.8 V; here the buffer is simulated at 1.8 V.</td>
</tr>
</tbody>
</table>
2.3.1 Types of I/O drivers/receivers

Table 4 lists the examples of the types of the I/O drivers and receivers.

Table 4  I/O drivers and receivers

<table>
<thead>
<tr>
<th>Type of I/O driver/receiver</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>c</td>
<td>CMOS type receiver</td>
</tr>
<tr>
<td>s</td>
<td>Schmitt type receiver (Schmitt is a type of CMOS receiver that has a hysteresis property while switching. It switches at different thresholds for low to high and high to low transitions.)</td>
</tr>
<tr>
<td>genout/genin</td>
<td>Direct in and out pads without any digital logic inside</td>
</tr>
<tr>
<td>nbnla nobscan_nolatch</td>
<td>nobscan (no boundary scan and no latch in the I/O)</td>
</tr>
<tr>
<td>nb</td>
<td>nobscan (no boundary scan macro in the I/O)</td>
</tr>
<tr>
<td>nl</td>
<td>nolvlsht (no level shifters in the I/O)</td>
</tr>
<tr>
<td>hv</td>
<td>High voltage</td>
</tr>
</tbody>
</table>

2.3.2 Drive strength

Table 5 lists the example drive strength used by the IBIS model in a naming convention.

Table 5  Drive strength examples

<table>
<thead>
<tr>
<th>Naming convention</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>216</td>
<td>The output driver strength varies from 2 mA to 16 mA.</td>
</tr>
<tr>
<td>47</td>
<td>The output driver strength varies from 4 mA to 7 mA.</td>
</tr>
<tr>
<td>28</td>
<td>The output driver strength varies from 2 mA to 8 mA.</td>
</tr>
</tbody>
</table>

2.3.3 Operating voltage

Supported operating voltages for I/O depend on the semiconductor process. The mostly used voltages are 2.8 V, 1.8 V, and 1.2 V.

2.3.4 Drive setting

Supported I/O drive strength is programmable, and it typically varies from 000 to 111, where 000 indicates the lowest drive, and 111 indicates the highest drive. This information can be extracted from the Model Selector section of an IBIS file.
A References

A.1 Acronyms and terms

<table>
<thead>
<tr>
<th>Acronym or term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>AMI</td>
<td>Algorithmic Modeling Information</td>
</tr>
<tr>
<td>CMOS</td>
<td>Complementary metal oxide semiconductor</td>
</tr>
<tr>
<td>GPIO</td>
<td>General-purpose I/O</td>
</tr>
<tr>
<td>hv</td>
<td>High voltage</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/output</td>
</tr>
<tr>
<td>I/V</td>
<td>Current/voltage</td>
</tr>
<tr>
<td>IBIS</td>
<td>I/O Buffer Information Specification</td>
</tr>
<tr>
<td>IC</td>
<td>Integrated circuit</td>
</tr>
<tr>
<td>nobscan</td>
<td>No boundary scan</td>
</tr>
<tr>
<td>nolatch</td>
<td>No latch</td>
</tr>
<tr>
<td>nolvlshft</td>
<td>No level shifter</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed circuit board</td>
</tr>
<tr>
<td>QTI</td>
<td>Qualcomm Technologies, Inc.</td>
</tr>
<tr>
<td>R, L, and C</td>
<td>Resistance, inductance, and capacitance</td>
</tr>
<tr>
<td>SI</td>
<td>Signal integrity</td>
</tr>
<tr>
<td>SPICE</td>
<td>Simulation Program with Integrated Circuit Emphasis</td>
</tr>
<tr>
<td>V/T</td>
<td>Voltage/time</td>
</tr>
</tbody>
</table>
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