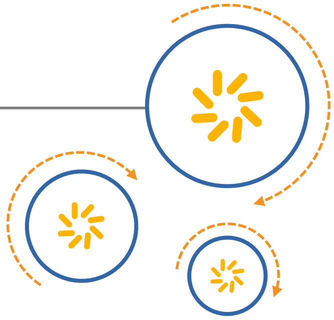
Qualcomm Technologies, Inc.



RB02

Hardware Reference Guide

80-YA116-19 Rev. A

July 3, 2017

Qualcomm Technologies, Inc.
5775 Morehouse Drive
San Diego, CA 92121
U.S.A.

Qualcomm Technologies, Inc. (“QTI”) and its affiliates reserve the right to make any updates, corrections and any other modifications to its documentation. The information provided in this document represents QTI’s knowledge and belief as of the date this document is provided. QTI makes no representation or warranty as to the accuracy of such information, and QTI assumes no liability for any use of the information in this documentation. You should obtain the latest information before placing orders for any hardware, and you should verify that such information is current and complete. Information published by QTI regarding any third-party products does not constitute a license to use such products or a warranty or endorsement thereof. Use of such information may require a license from a third party under the intellectual property rights of such third party, or a license from QTI or its affiliates under the intellectual property rights of QTI or its affiliates.

All hardware, equipment, components or products are sold subject to QTI’s (or such other QTI affiliated company that is designated by QTI) standard terms and conditions of sale, as applicable. Notwithstanding anything to the contrary in this documentation or otherwise: (i) you do not receive any rights, licenses, or immunities from suit under any patents of Qualcomm Incorporated, QTI or their respective affiliates as a result of receiving this documentation (whether expressly, impliedly, by virtue of estoppel or exhaustion, or otherwise), (ii) without limitation, you shall not use or sell any wireless wide area network (“WWAN”) baseband integrated circuit that you purchase or acquire from QTI or any product that incorporates any such WWAN baseband integrated circuit (whether alone or in combination with any other software or components) without a separate license or non-assertion covenant from Qualcomm Incorporated in respect of or under all applicable patents, (iii) nothing in this document modifies or abrogates your obligations under any license or other agreement between you and Qualcomm Incorporated, including without limitation any obligation to pay any royalties, and (iv) you will not contend that you have obtained any right, license, or immunity from suit with respect to any patents of Qualcomm Incorporated, QTI or their respective affiliates under or as a result of receiving this documentation (whether expressly, impliedly, by virtue of estoppel or exhaustion, or otherwise).

Revision history

Revision	Date	Description
A	July 2017	Initial release

Contents

Figures

Tables

1 Introduction

The RB02 board brings out all interfaces supported by QCA4010 in minimal PCB form factor. The RB02 interfaces can be easily and safely accessed via RB01. The functional mode of RB02 board is decided by the bootstrap configuration on RB01, which meanwhile facilitates evaluation of QCA4010 power consumption and Wi-Fi performance.

The combination of RB02 and RB01 forming an evaluation platform can also be used for software development of QCA4010-based systems.

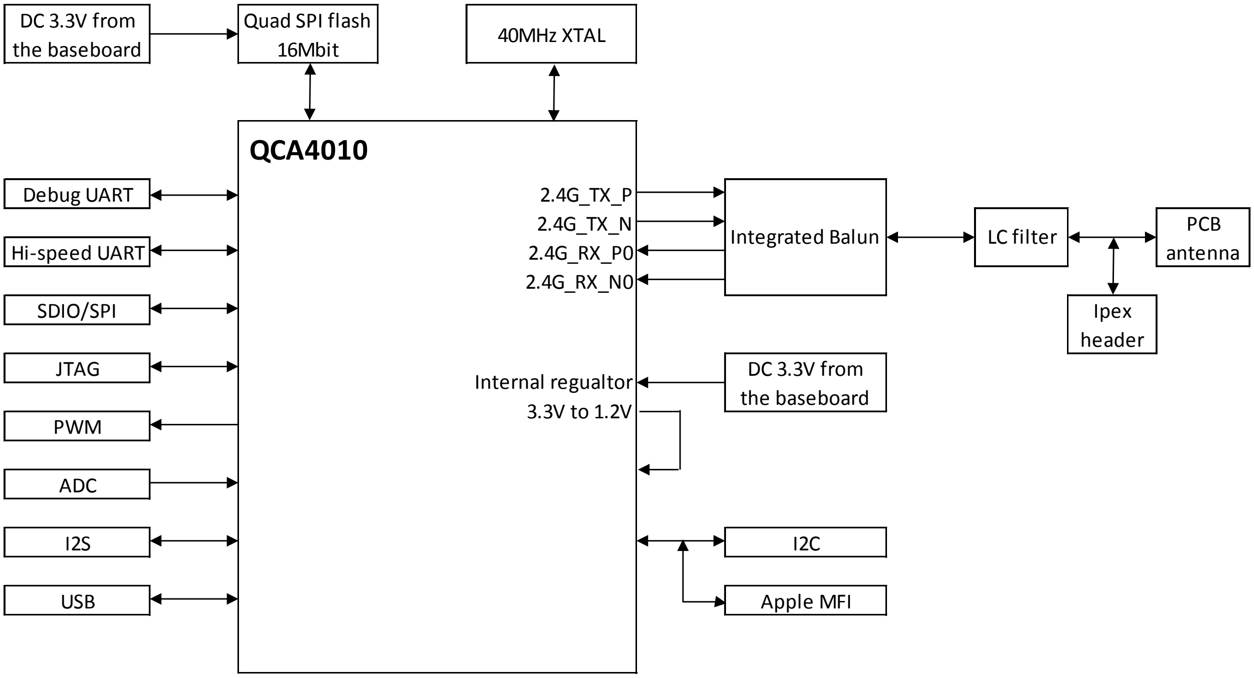


Figure 1-1 RB02 block diagram

2 RB02 component and interface

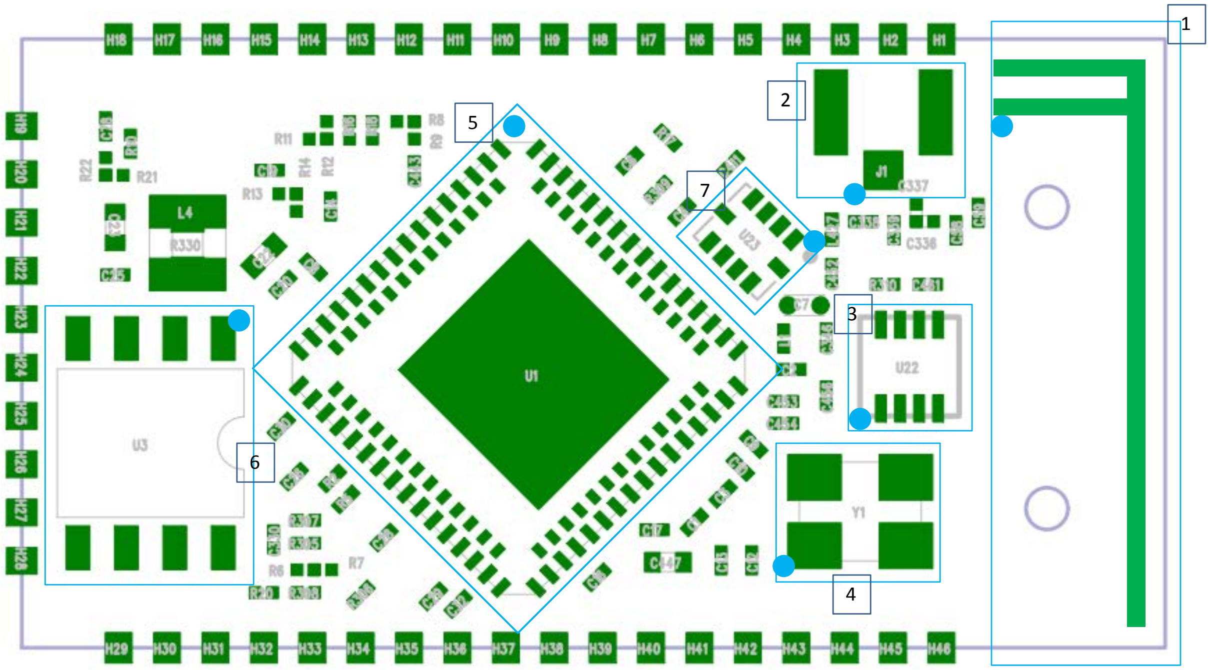


Figure 2-1 RB02 reference design module (front view)

NOTE: The picture is for reference only.

Table 2-1 RB02 details

1	2.4 GHz Printed Antenna
2	Tx/Rx RF Ipex Conn
3	Apple MFI
4	40 MHz Crystal
5	QCA4010 Area
6	16 Mbit Quad SPI Flash
7	Integrated Balun

2.1 RB02 main components

Table 2-2 lists the components contained in RB02.

Table 2-2 Components list

Component	Description
2.4 GHz Printed Antenna	Printed Inverted F Antenna for 2.4 GHz Band
Tx/Rx RF Ipex Connector	RF Connector for Transmitting and Receiving RF signal measurement
Apple MFI	Apple MFI certification IC
40 MHz Crystal	Provide 40 MHz Reference Clock
QCA4010	Refer to QCA4010 Device Specification
SPI Flash	The 16 Mbit SPI flash supports quad mode
Integrated Balun	Single Balun IC to minimize cost, size, tuning and tolerance

2.2 RB02 RF section

The RF section contains 2.4 GHz RF Balun, Band-trap Filter, RF Matching Circuit.

2.3 RB02 interface

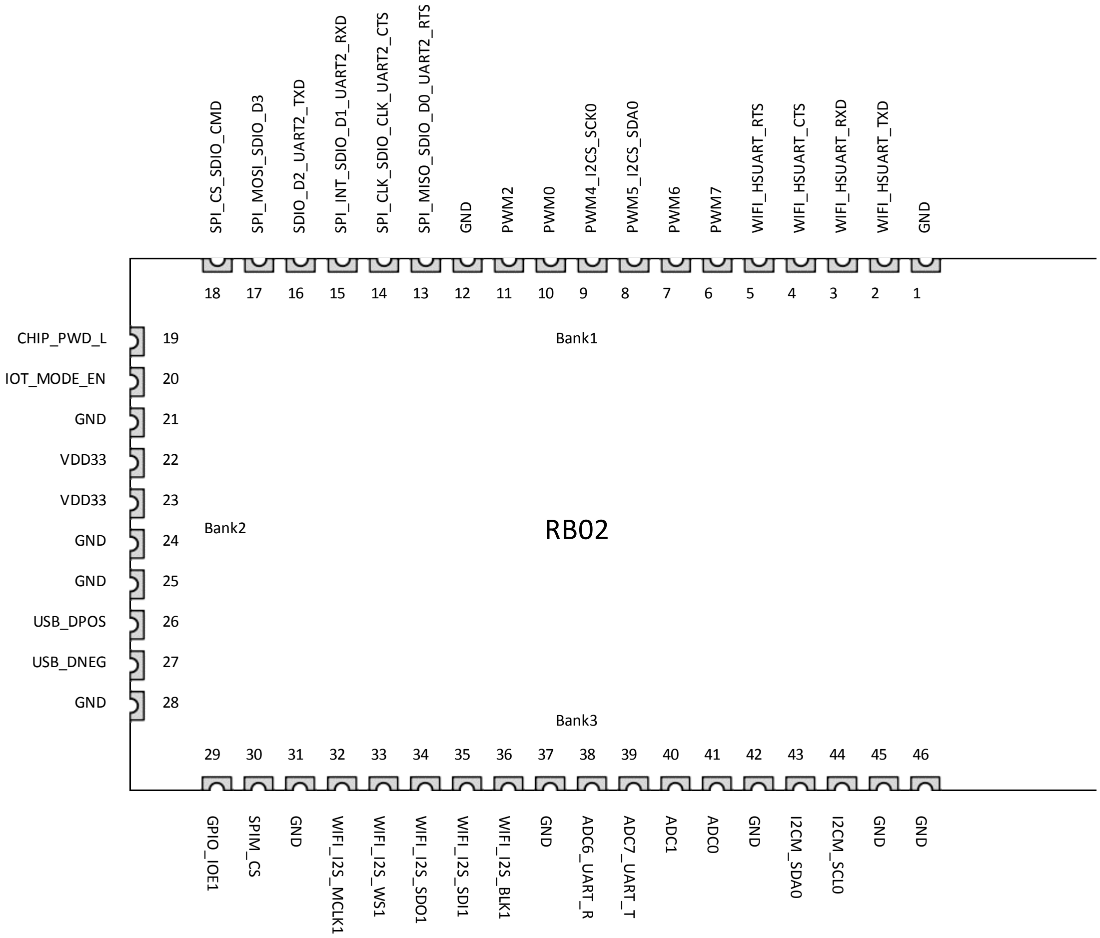


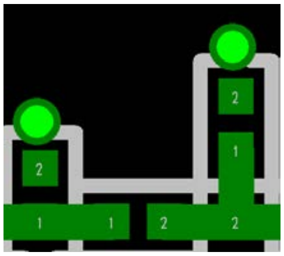
Figure 2-2 RB02 module interface definition (top view)

3 Design guidelines for the RB02

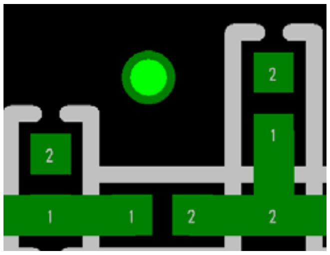
3.1 GND

3.1.1 Placement of capacitor shunted to GND

- Place bypass capacitors as close to the respective pins as possible.
- Place at least one dedicated ground via for each capacitor shunted to ground and put ground via as close to the capacitors as possible:



Good capacitor placement (2 capacitors with 2 dedicated ground vias)



Bad capacitor placement (2 capacitors sharing only 1 ground via)

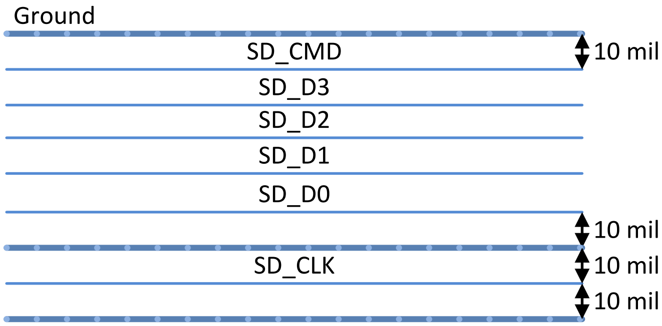
3.1.2 GND

Avoid large ground planes without ground vias. The ground plan shown in Figure 3-1 can act like an antenna radiating unwanted signals to other parts of the reference board.

Figure 3-1 Example: ground plane without ground vias

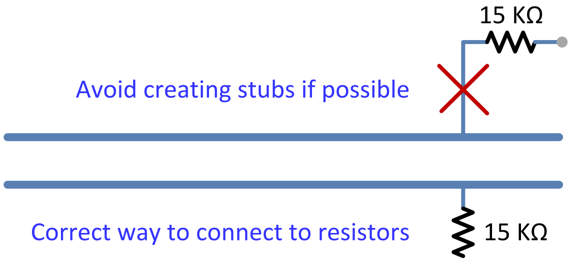
3.1.3 SDIO

- Use ground trace for SDIO routing to isolate SD_CLK.
- Avoid routing parallel to SD_CLK (above, underneath and on both sides); SD_CLK can run up to 50 MHz and can couple to other traces.
- Keep the reference ground plan of SDIO lines as solid as possible.
- Route SDIO lines on inner layers to avoid picking up noise.



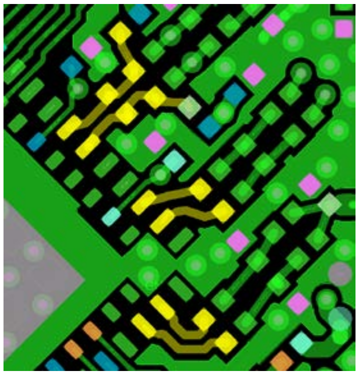
3.2 USB

- Use 90 Ω differential lines to rout USB D+/D-.
- Avoid routing USB lines close to the edge of the board.
- Avoid routing USB lines with 90° turns. Use 45° transition.
- Avoid placing stub components on the USB data lines.

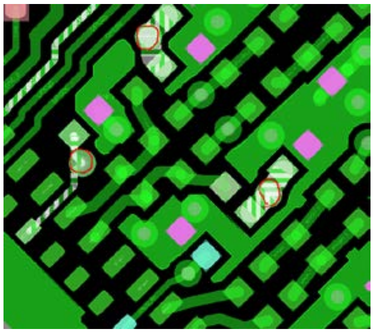


3.3 RF routing

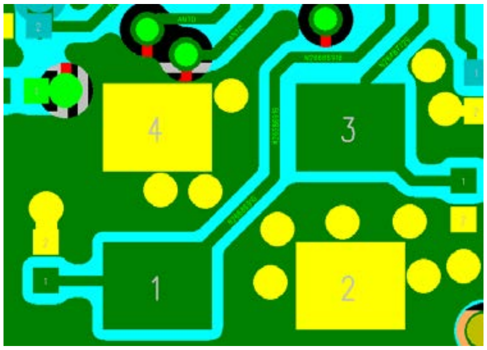
- Route all differential and single-ended traces for RF signal with an impedance of 50 Ω. Avoid right angle line routing.
- Keep the length of the RF differential output traces as short as possible.



- Use separate vias to tie all the power pins to the power traces or power plane. Do not make the power pins share the same VDD via.



- Avoid power trace routing underneath the QCA4010.
- Enclose the crystal traces with ground plane and avoid routing power traces underneath the crystal.



- If power planes are used, avoid via holes as they will break the integrity of the power plan. Figure 3-2 shows how via holes can block the current path on the power plan.

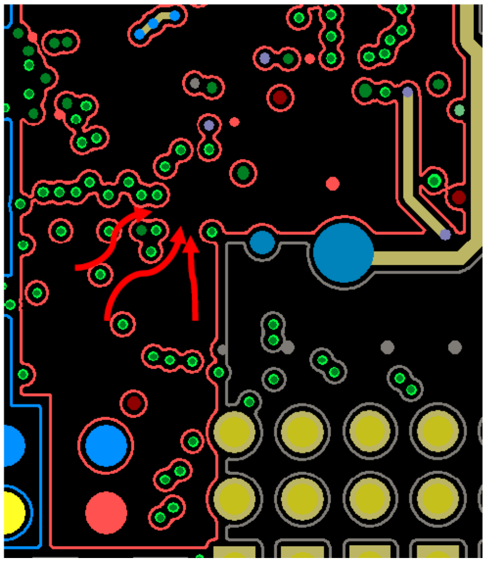


Figure 3-2 Example: via holes blocking the current path on the power plan

3.4 Board stack-up

The RB02 reference design is implemented on a four-layer board:

- Layer 1 is for RF and signal traces.
- Layer 2 is the ground plan.
- Layer 3 is for power and signal.
- Layer 4 is for signal and ground.

The RB02 consists of the elements listed in this section with the board stack-up as shown in Table 3-1.

- 4-layer board
- Total stack thickness: 39.8 mil/1 mm
- Material: FR4 Tg 140
- Dielectric constant 4.25 @ 5 GHz

Table 3-1 RB02 reference design board stack-up

4 layer stack-up for 1 mm +/- 0.15mm board thickness			Thickness (mil)	Thickness (mm)
		Solder mask	0.7	0.018
L1	PTH 1-4	Copper foil 0.333oz + Plating	1.2	0.03
FR4		Core 2.8mil	2.8	0.071
L2		Copper foil 0.5oz	0.65	0.0165
FR4		Core 28mil	28	0.711
L3		Copper foil 0.5oz	0.65	0.0165
FR4		Core 2.8mil	2.8	0.071
L4		Copper foil 0.333oz + Plating	1.2	0.03
		Solder mask	0.7	0.018
Total			38.7	0.982