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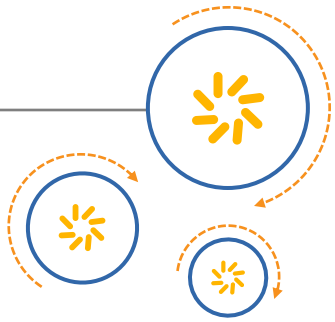

RB01 Development Platform Hardware

User Guide

80-YA116-13 Rev. A

February 3, 2017

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Revision history

Revision	Date	Description
A	February 2017	Initial release

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Tables

1 RB01 Development Platform

RB01 development platform provides mode configuration, interface extension, peripheral access and power supply for RB02 and RB04 modules. Different boot and function modes of RB02/RB04 module are configured on the RB01. Most RB02/RB04 module interfaces can be accessed on the RB01 board with buffer protection. The RB01 can also be used for module manufacturing test.

1.1 RB01 layout and interfaces

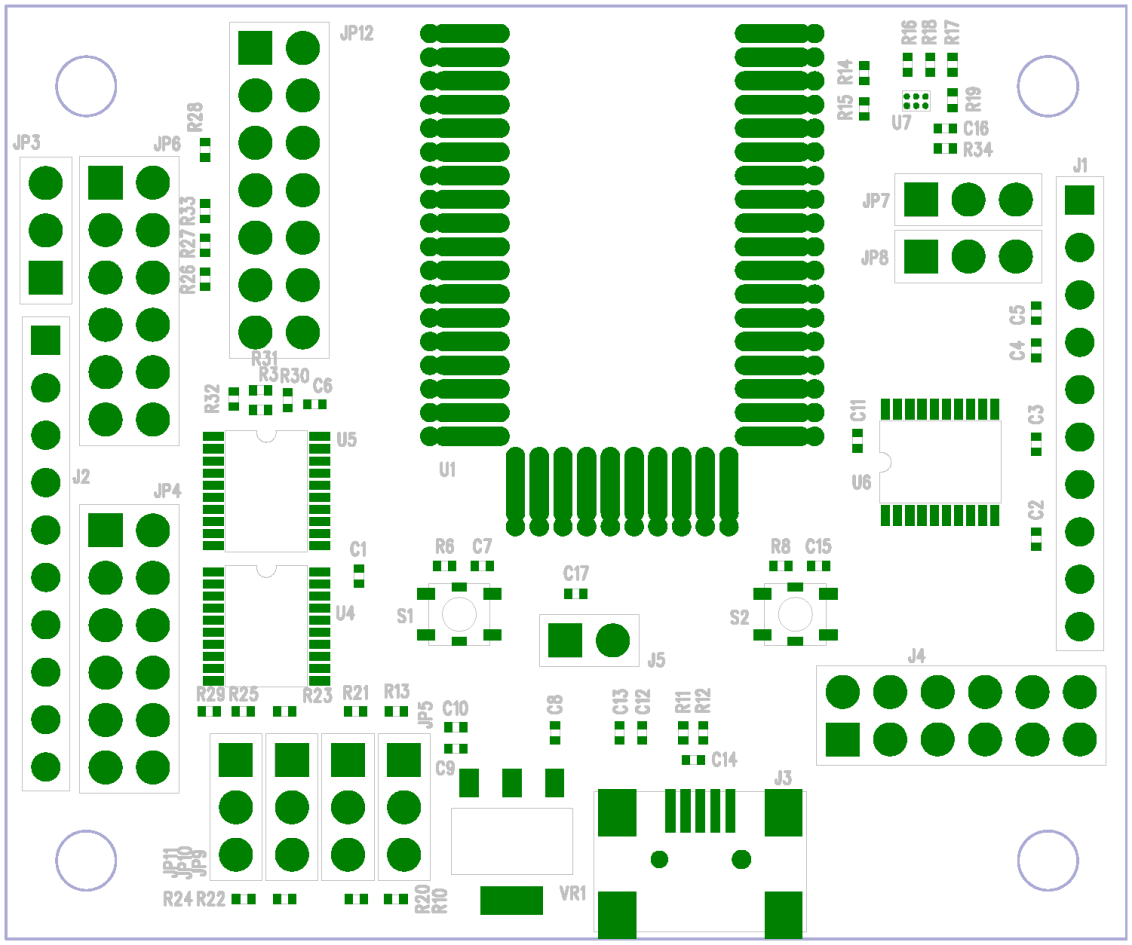

Figure 1-1 RB01 development platform (front view)

Table 1-1 RB01 components

J2	PWM x 6, I^2C slave x 1	**U1**	RB02 or RB04 module
JP6	Hi-speed UART of RB02; GPIO x 3 of RB04	**J3**	Mini-USB interface, for ART and power supply
JP4	SPI x 1, SDIO x 1 or Hi-speed UART of RB02; BT PCM interface of RB04	**U7**	I^2C thermal sensor TMP106
J4	I^2S interface	**JP3**	MP1 hi-speed UART routing
J1	ADC x 4, debug UART x 1	**JP11**	Test mode bootstrap
JP7, JP8	I^2C master interface header	**JP10**	Host mode bootstrap
VR1	5 V-to-3.3 V LDO	**JP9**	Host mode bootstrap
J5	3.3 V power jumper for RB02/RB04	**JP5**	IOT mode bootstrap
S1	RB02/RB04 module reset, active low	**S2**	RB02/RB04 module wakeup, active low
JP12	JTAG header	**U4, U5, U6**	Octal FET bus switch

1.2 RB01 functionality

This section lists the power supply, jumper settings, push button, headers interfaces and their pin assignments.

Table 1-2 Power supply

Component	Definition and description
J3	Mini-USB interface, for ART and power supply
VR1	LDO, 5 V to 3.3 V convertor
J5	J5.1 is output from VR1, J5.2 is the power rail for RB02/RB04 Module. Connect J5.1 & J5.2 when using LDO power rail to RB02/RB04 Module.

Table 1-3 Jumper settings

Jumper	Pin no.	Definition and description	Usage
JP3	JP3.1	Hi-speed UART TXD (only for RB02)	For RB02, connect JP3.1 & JP3.2; For RB04, connect JP3.3 & JP3.2
	JP3.2	RB02/RB04 module pin2	
	JP3.3	Ground	
JP11	JP11.1	Ground, logic low = 0	For normal operation, connect JP11.1 & JP11.2
	JP11.2	GPIO[8], bootstrap test mode enable	
	JP11.3	+3.3V, logic high = 1	
JP10	JP10.1	Ground, logic low = 0	For USB mode: connect JP10.1 & JP10.2, JP9.1 & JP9.2 For UART/hostless mode: connect JP10.3 & JP10.2, JP9.1 & JP9.2 For SPI hosted mode: connect JP10.1 & JP10.2, JP9.3 & JP9.2 For SDIO hosted mode: connect JP10.3 & JP10.2, JP9.3 & JP9.2
	JP10.2	GPIO[4], bootstrap host mode 0	
	JP10.3	+3.3V, logic high = 1	
JP9	JP9.1	Ground, logic low = 0	
	JP9.2	GPIO[0], bootstrap host mode 1	
	JP9.3	+3.3V, logic high = 1	

Jumper	Pin no.	Definition and description	Usage
JP5	JP5.1	Ground, logic low = 0	For normal operation, connect JP5.3 & JP5.2
	JP5.2	Bootstrap IOT mode enable	
	JP5.3	+3.3 V, logic high = 1	

Table 1-4 Push button

Push button	Definition and description
S1	RB02/RB04 module reset, active low
S2	RB02/RB04 module wakeup, active low

Table 1-5 Header interfaces

Header	Pin no.	Function1	Function2	Function3	Function4	QCA401x GPIO no.
J2	J2.1	Ground				
	J2.2	PWM7				GPIO[13]
	J2.3	PWM6				GPIO[12]
	J2.4	Ground				
	J2.5	PWM4	I2C slave clock			GPIO[10]
	J2.6	PWM5	I2C slave data			GPIO[11]
	J2.7	Ground				
	J2.8	PWM2				GPIO[8]
	J2.9	PWM0				GPIO[6]
	J2.10	Ground				
JP6	JP6.1	Ground				
	JP6.2	Ground				
	JP6.3	Ground				
	JP6.4	Hi-speed UART TXD (RB02)				GPIO[24] (RB02)
	JP6.5	Ground				
	JP6.6	Hi-speed UART RXD (RB02)	GPIO[17] (RB04)			GPIO[23] (RB02)
	JP6.7	Ground				
	JP6.8	Hi-speed UART CTS (RB02)	GPIO[18] (RB04)			GPIO[22] (RB02)
	JP6.9	Ground				
	JP6.10	Hi-speed UART RTS (RB02)	GPIO[19] (RB04)			GPIO[21] (RB02)
	JP6.11	Ground				
	JP6.12	Ground				
J4	J4.1	+5.0V power supply				

Header	Pin no.	Function1	Function2	Function3	Function4	QCA401x GPIO no.
	J4.2	3.3V Power				
	J4.3	I2S main clock				GPIO[33]
	J4.4	Ground				
	J4.5	I2S WS				GPIO[32]
	J4.6	Ground				
	J4.7	I2S SDO				GPIO[31]
	J4.8	Ground				
	J4.9	I2S SDI				GPIO[30]
	J4.10	Ground				
	J4.11	I2S bit clock				GPIO[27]
	J4.12	Ground				
J1	J1.1	Ground				
	J1.2	ADC0				
	J1.3	Ground				
	J1.4	ADC1				
	J1.5	Ground				
	J1.6	ADC7	Debug UART TXD			GPIO[28]
	J1.7	Ground				
	J1.8	ADC6	Debug UART RXD			GPIO[29]
	J1.9	Ground				
	J1.10	Module flash /CS pin				GPIO[35]
JP7	JP7.1	I2C master clock				GPIO[26]
	JP7.2	I2C master data				GPIO[25]
	JP7.3	Ground				
JP8	JP8.1	I2C master clock				GPIO[26]
	JP8.2	I2C master data				GPIO[25]
	JP8.3	Ground				
J5	J5.1	+3.3V power rail				
	J5.2	+3.3V power rail				
JP4	JP4.1	Ground				
	JP4.2	SPI MISO (RB02)	SDIO Data0 (RB02)	Hi-speed UART RTS (RB02)		GPIO[4]
	JP4.3	Ground				
	JP4.4	SPI clock (RB02)	SDIO clock (RB02)	Hi-speed UART CTS (RB02)	BT PCM bit clk (RB04)	GPIO[5] (RB02)
	JP4.5	Ground				
	JP4.6	SPI interrupt (RB02)	SDIO data1 (RB02)	Hi-speed UART RXD (RB02)	BT PCM Sync (RB04)	GPIO[3] (RB02)
	JP4.7	Ground				
	JP4.8	Ground	SDIO data2 (RB02)	Hi-speed UART TXD (RB02)	BT PCM input (RB04)	GPIO[2] (RB02)

Header	Pin no.	Function1	Function2	Function3	Function4	QCA401x GPIO no.
	JP4.9	Ground				
	JP4.10	SPI MOSI (RB02)	SDIO data3 (RB02)		BT PCM output (RB04)	GPIO[1] (RB02)
	JP4.11	Ground				
	JP4.12	SPI Chip select (RB02)	SDIO CMD (RB02)			GPIO[0]
JP12	JP12.1	TDI				GPIO[6]
	JP12.2	GND				
	JP12.3	TDO				GPIO[13]
	JP12.4	GND				
	JP12.5	TCK				GPIO[12]
	JP12.6	GND				
	JP12.7	NC				
	JP12.8	GND				
	JP12.9	TRST				GPIO[19]
	JP12.10	TMS				GPIO[10]
	JP12.11	TVCC				
	JP12.12	NC				
	JP12.13	NC				
	JP12.14	RESET				

NOTE:

- (RB02) indicates interface available when RB02 module installed on the RB01.
- (RB04) indicates interface available when RB04 module installed on the RB01.

Table 1-6 I²C sensor

Component	Definition and description	QCA401x GPIO no.
U7	I²C thermal sensor	
	TMP106	
	U7.A1: I2C_SDA	GPIO[25]
	U7.B1: I2C_SCL	GPIO[26]
	U7.B2: ALERT	GPIO[13]

2 PCB Design Guidelines

2.1 GND

2.1.1 Placement of capacitor shunted to GND

- Place bypass capacitors as close to the respective pins as possible.
- Place at least one dedicated ground via for each capacitor shunted to ground and put ground via as close to the capacitors as possible.

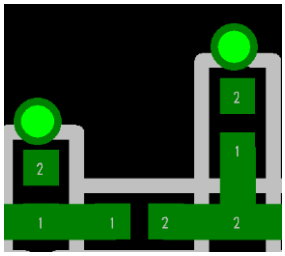

Figure 2-1 Good capacitor placement (2 capacitors with 2 dedicated ground vias)

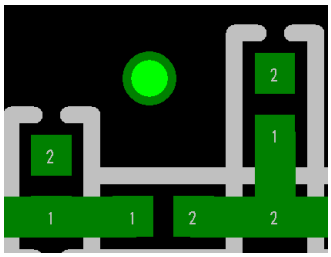

Figure 2-2 Bad capacitor placement (2 capacitors sharing only 1 ground via)

2.1.2 GND

Avoid large ground planes without ground vias. The ground plane shown in Figure 2-1 can act like an antenna radiating unwanted signals to other parts of the reference board.

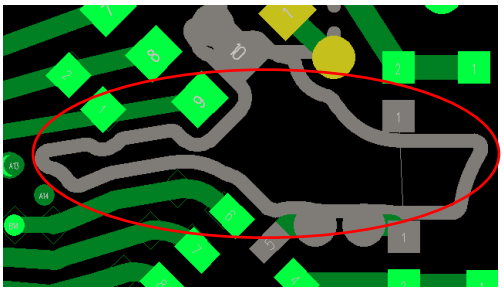

Figure 2-13 Ground plane without ground vias

2.1.3 SDIO

- Use a ground trace for SDIO routing to isolate SD_CLK.
- Avoid routing parallel to SD_CLK (above, underneath, and on both sides); SD_CLK can run up to 50 MHz and can couple to other traces.
- Keep the reference ground plane of SDIO lines as solid as possible.
- Route SDIO lines on inner layers to avoid picking up noise.

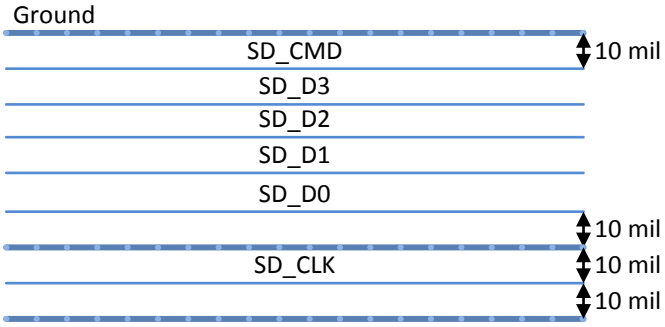

Figure 2-4 SDIO Signal Stack-up

2.2 USB

- Use 90 Ω differential lines to rout USB D+/D-.
- Avoid routing USB lines close to the edge of the board.
- Avoid routing USB lines with 90º turns. Use 45° transition.
- Avoid placing stub components on the USB data lines.

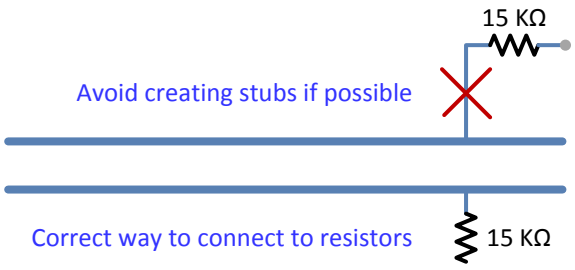

Figure 2-5 USB Recommendation

2.3 RF design for Wi-Fi modules

This section is more related to the Wi-Fi modules than to the RB01.

- Route all differential and single-ended traces for RF signal with an impedance of 50 Ω. Avoid right angle line routing. Qualcomm Technologies recommends all RF components and traces to be on the same side of the board.
- Avoid vias as much as possible in the RF traces. Do not use any test points on any RF traces or component.
- Minimize the length of all RF traces since FR4 material incurs losses at RF frequencies. Minimizing the trace length reduces the overall signal loss. Keeping the Tx path short is more important than keeping the Rx path short.
- A loss in signal strength in the Tx path cannot be recovered, but the Rx signal can be amplified on-board, to compensate for loss.
- Do not put metal under the U.FL connectors on layer 1. Make sure that the ground is present on all other layers of the board.
- Keep the length of the RF differential output traces as short as possible.

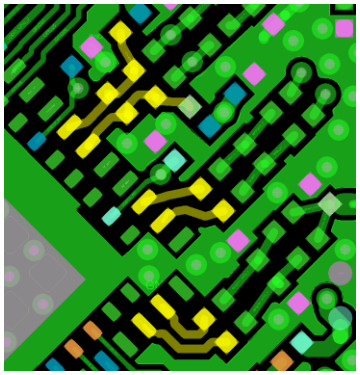

Figure 2-6 RF Differencial Traces

- Use separate vias to tie all the power pins to the power traces or power plane. Do not make the power pins share the same VDD via.

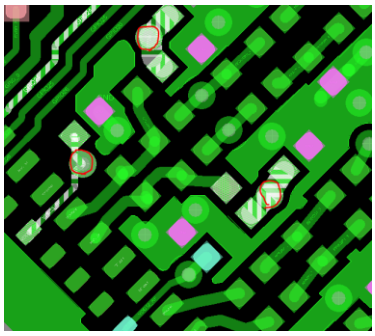

Figure 2-7 Power Pin Vias

- Avoid power trace routing underneath the QCA4010/QCA4012.

- Enclose the crystal traces with ground plane and avoid routing power traces underneath the crystal.

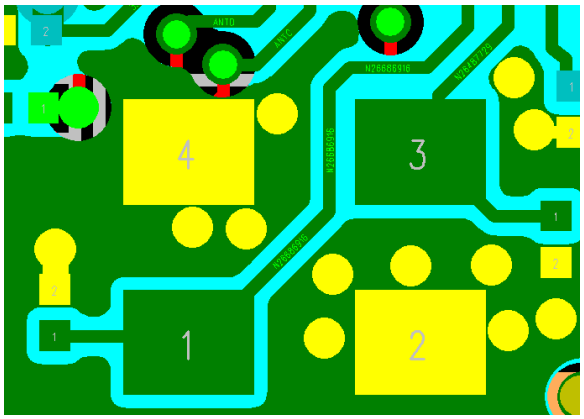

Figure 2-8 Crystal Traces

- If power planes are used, avoid via holes badly breaking the integrity of the power plane. The following figure shows how via holes can block the current path on the power plane.

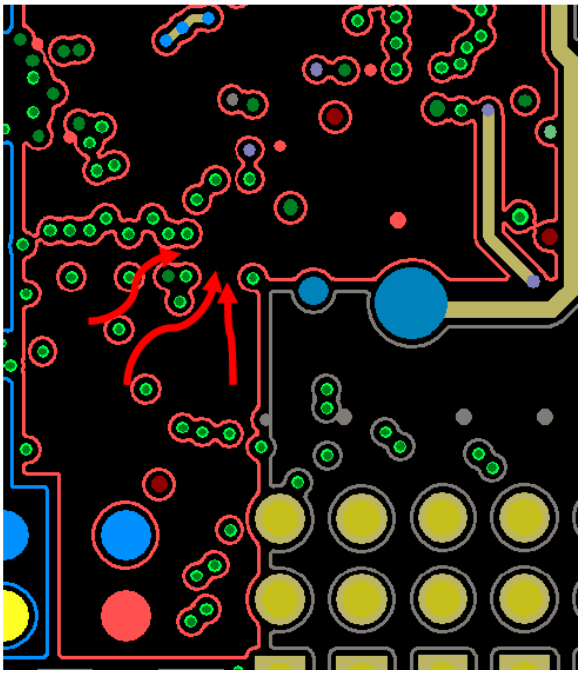

Figure 2-9 Example: Via holes blocking the current path on the power plane

2.4 Board stack-up

The RB01 is implemented on a two-layer board:

- Layer 1 is for signal traces.
- Layer 2 is mainly ground plane.

The RB01 is comprised of the elements listed in this section, with the board stack-up as shown in Figure 2-2.

- 2-layer board
- Total stack thickness: 63 mil/1.6 mm
- Material: FR4 Tg 140
- Dielectric constant @ 5 GHz: 4.25
- Impedance @ 2.4 GHz: 50 Ω

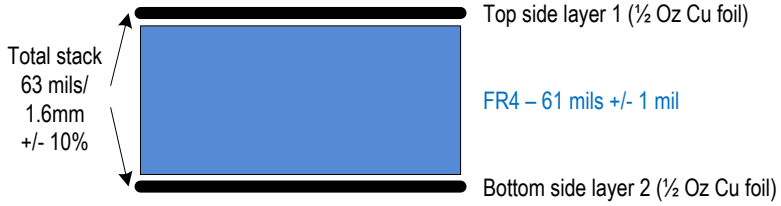

Figure 2-210 RB01 board stack-up