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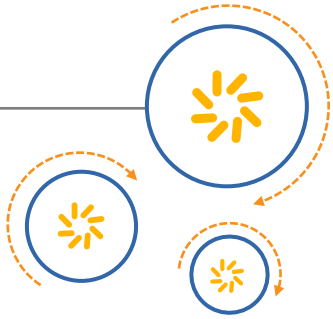

WCN3620 Wireless Connectivity IC Design Guidelines

September 2016

Questions or comments: https://developer.qualcomm.com/forums/qdn-forums/hardware

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Revision	Date	Description
B	September 2016	Update to ‘E’ part
A	August 7, 2015	Initial release

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1 Introduction

1.1 Purpose

This document provides an overview of the WCN3620 wireless connectivity IC design; its capabilities, components, and interfaces.

1.2 Acronyms, abbreviations, and terms

Table 1-1 provides definitions for the acronyms, abbreviations, and terms used in this document.

Table 1-1 Acronyms, abbreviations, and terms

Term	Definition
ACL	Asynchronous Connection-Less
ADC	Analog-to-Digital Converter
AHB	Advanced High-Performance Bus
API	Application Programming Interface
uAPSD	Unscheduled Automatic Power Save Delivery
ARM	Advanced Risk Machines
AXI	Advanced eXtensible Interface
BB	Baseband
BPF	Bandpass Filter
BR	Basic Rate
BT	Bluetooth
CLPC	Closed-loop power control
CMOS	Complementary Metal Oxide Semiconductor
COM	Communication
DAC	Digital-to-Analog Converter
DDR	Double Data Rate
DMA	Direct Memory Access
EBT	Early Burst termination
EDR	Enhanced Data Rate
FM	Frequency Modulation
GFSK	Gaussian Frequency Shift Keying
HKADC	House Keeping Analog to Digital Converter
IC	Integrated Circuit

Term	Definition
JTAG	Joint Test Action Group
LE	Low Energy
LO	Local Oscillator
LPASS	Low Power Audio Sub System
LPO	Low power oscillator
LPPS	Low Power Page Scan
LNA	Low Noise Amplifier
MAC	Message Authentication Code
MMSS	Multimode System Selection
NVM	Non Volatile Memory
PA	Power Amplifier
PMIC	Power Management Integrated Circuit
ROM	Read Only Memory
RF	Radio Frequency
RPM	Resource and Power Manager
RZ	Return-to-zero
SCO	Synchronous Connection Oriented link
SDI	Standard Disk Interconnect
SCPC	Self-calibrating power control
SPM	System Power Manager
SSBI	Synchronous-System Bus Interference
TLMM	top-level mode multiplexer
Tx	Transmission
uAPSD	Unscheduled automatic power-save delivery
VSWR	Voltage Standing Wave Ratio
WCSS	Wireless Connectivity Sub System
WLAN	Wide Local Area Network
WLNSP	Wafer Level Nano Scale Package

2 Wireless Connectivity System Overview

2.1 WLAN + Bluetooth + FM radio system introduction

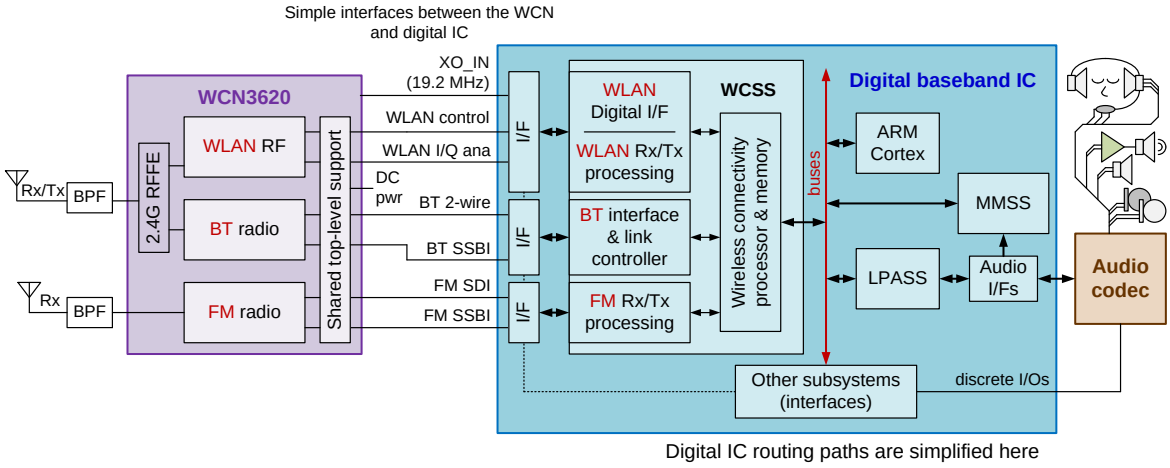

Figure 2-1 WLAN + Bluetooth + FM radio system introduction

- WLAN supports 2.4 GHz
- Bluetooth (BT) shares the WLAN 2.4 GHz front-end
- FM Rx-only uses headset wiring as an antenna
- All RF transceiver circuits are integrated into the WCN3620

In addition to digital processing for WLAN/BT/FM, the digital IC provides:

- Interfaces with the WCN (analog baseband and various serial digital interfaces)
- Buses for routing between digital IC subsystems and external ports
- Microprocessor subsystem for processing power (ARM® Cortex in the example shown)
- Low power audio subsystem and audio interfaces with the audio codec IC
- Multimedia subsystem or camera, video, and graphics support
- Other subsystems for peripheral connectivity, memory, etc.

2.2 Summary of WCN3620 features

Table 2-1 Summary of WCN3620 features

Feature	WCN3620 capability
System-level	
Highly integrated	Integrated WLAN, BT, and FM radio RF functionality Lower parts count and less PCB area overall Eliminates external PA, LNA matching, and antenna Tx/Rx switching
WLAN + BT	Concurrent reception in the 2.4 GHz band PTA
Automated calibration	No external equipment required
Top-level support circuits	
Clock	External source: 19.2 MHz Clock buffering, gating, and distribution to all other blocks
Digital IC interfaces	Manages all WLAN, Bluetooth, and FM interfaces
DC power	Gates and distributes power to all other blocks
WLAN RF (with baseband IC digital processing)	
Single-band support	2.4 GHz RF transceiver Concurrent WLAN + BT reception in 2.4 GHz band
Simple host interfaces	4-line analog baseband interface with Rx/Tx multiplexing
IEEE 802.11 compliance	b/g/n with companion digital IC
Integrated PAs and LNAs	High dynamic Tx power & excellent Rx sensitivity for extended range
Other solution-level features	Wake-on-WLAN (WoWLAN) support MCS 0, 1, 2, 3, 4, 5, 6, and 7; up to 72 Mbps data rate Space-time block coding (STBC) support A-MPDU reception/retransmission and A-MSDU reception Support for A-MPDU aggregation Support for short guard interval Infrastructure and ad-hoc operating modes SMS4 hardware encryption (for WAPI support) AP-mode hardware support Wi-Fi direct
Bluetooth radio	
Bluetooth specification compliance	BT 4.0 HS low energy 4.0 compliant; 1.x, 2.x + EDR, and 3.0 backward compatible
Highly integrated	Baseband modem and 2.4 GHz transceiver; improved Rx sensitivity
Simple host interfaces	2-line digital data interface supports Rx and Tx SSBI for status and control
Supported modulation	GFSK, π/4-DQPSK, and 8-DPSK (in both directions)
Connectivity	Up to 7 total wireless connections Up to 3.5 piconets (master, slave, and page scanning) One SCO or eSCO connection
Digital processing	Support for BT + WLAN coexistence, including concurrent receive Support for all BR, EDR, and BLE packet types

Feature	WCN3620 capability
RF Tx power levels	Class 1 & 2 power-level transmissions without external PA
FM radio	
Worldwide FM band support	76 to 108 MHz, with 50 kHz channel spacing
Highly integrated	Baseband processing and RF transceiver Data system support Radio data system for Europe (RDS) Radio broadcast data system for USA (RBDS)
Simple host interfaces	Single-line digital data interface SSBI for status and control
Rx support	External wired-headset antenna Rx operation simultaneously with a phone connection
Highly automated	Search and seek; gain control; frequency control; noise cancellation; soft mute; high-cut control; mono/stereo blend; adjustment-free stereo decoder; programmable de-emphasis
Fabrication technology and package	
Single die	65 nm CMOS
Small, thermal efficient pkg	61 WLNSP: 3.32 × 3.55 × 0.63 mm; 0.40 mm pitch

2.3 Wireless connectivity system detailed block diagram

The three major subsystems – WLAN, Bluetooth, and FM radio – are split between the two ICs

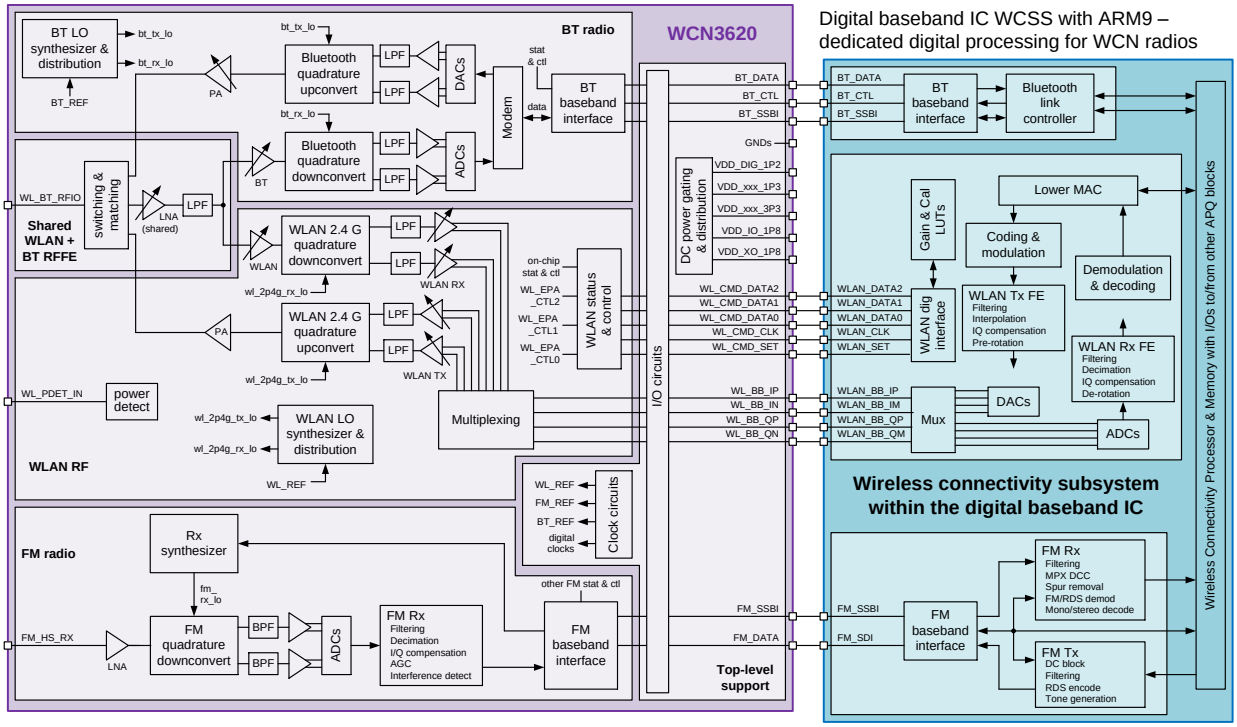

Figure 2-2 Three major subsystems

2.4 Wireless connectivity specific reference documents

- LM80-P0436-25 WCN3620 Wireless Connectivity IC Design Guidelines (this document)
- LM80-P0436-26 WCN3620 Layout Guidelines
- LM80-P0436-27 WCN3620 Wireless Connectivity Reference Schematic
- LM80-P0436-28 WCN3620 Wireless Connectivity Design Example with 2G FEM + External Coupler
- LM80-P0436-32 WCN3620 Wireless Connectivity IC Device Revision Guide
- LM80-P0436-33 WCN3620 Wireless Connectivity IC Device Specification (Advance Information)

NOTE: This list may contain documents that have not yet been released. The document numbers and titles are subject to change.

3 WCN3620 Wireless Local Area Network

3.1 External coupler and discrete power detector

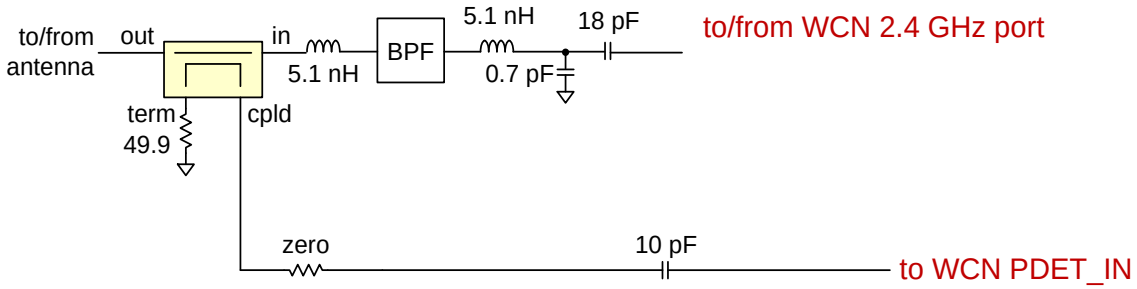

Figure 3-1 External coupler and discrete power detector

3.2 Tx power control options (CLPC and SCPC)

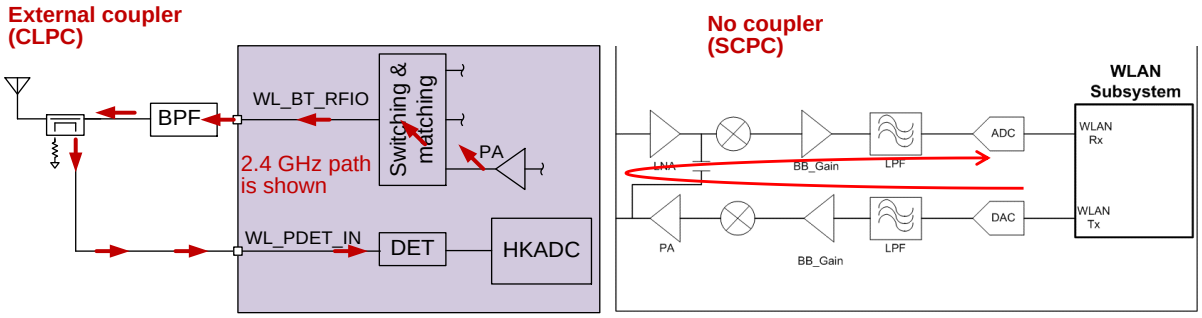

Figure 3-2 CLPC and SCPC

- The Tx power detection mechanism monitors the output power level on a frame-by-frame basis, ensuring emissions and EVM requirements are met.
- There are two choices for Tx power control and each requires bench characterization:
  - Closed-loop power control (CLPC)
    - Requires additional external coupler + power detect circuit BoM.
  - Self-calibrating power control (SCPC)
    - No external circuit required.
    - Less dependent on external loading. Has no packet-to-packet variation.

3.3 SCPC

SCPC is an automatic initialization method that includes an on-chip gain adjustment routine to reduce Tx output power variation.

SCPC uses existing digital pre-distortion (DPD) calibration information, which is run at cold boot.

- Saturated PA (PSAT) power has very little (<1 dB) variation from part to part.
- PSAT used as a reference to determine target power.
- Runs in an open loop after part output power is determined.
- Uses information already obtained during DPD calibration, which uses Tx/Rx loopback.
- Adjusts output power gain settings on a packet-by-packet basis.
- SCPC loopback path does not include external power detector circuitry or the internal power detector.
- Open loop power control does not react to external loading or mismatch.
- Open loop power control shows more consistent packet-to-packet power control.

3.4 WLAN analog baseband interface – schematic

- Multiplexing within WCN3620 and digital baseband ICs allows the same two differential pairs (I and Q) to be used in both directions –Tx and Rx.
- The bandwidth is 20 MHz.
- Very sensitive I and Q baseband signals have tight linearity requirements with limited Rx drive capability.
- Route as phase-critical differential pairs –equal lengths.
- Keep signals three-line widths or greater away from each other.
- Resistance and capacitance on each pair should be equal; total capacitance should be less than 10 pF. Routing impedance is not critical, but 60 to 70 Ω is recommended to minimize capacitive loading.
- Crosstalk should be less than 60 dB at 50 MHz (goal).
- Isolate from digital logic and clocks with ground all around; treat similar to a controlled-impedance stripline. Route on inner layers and transition to outer layers at ICs as quickly as possible to minimize capacitance.

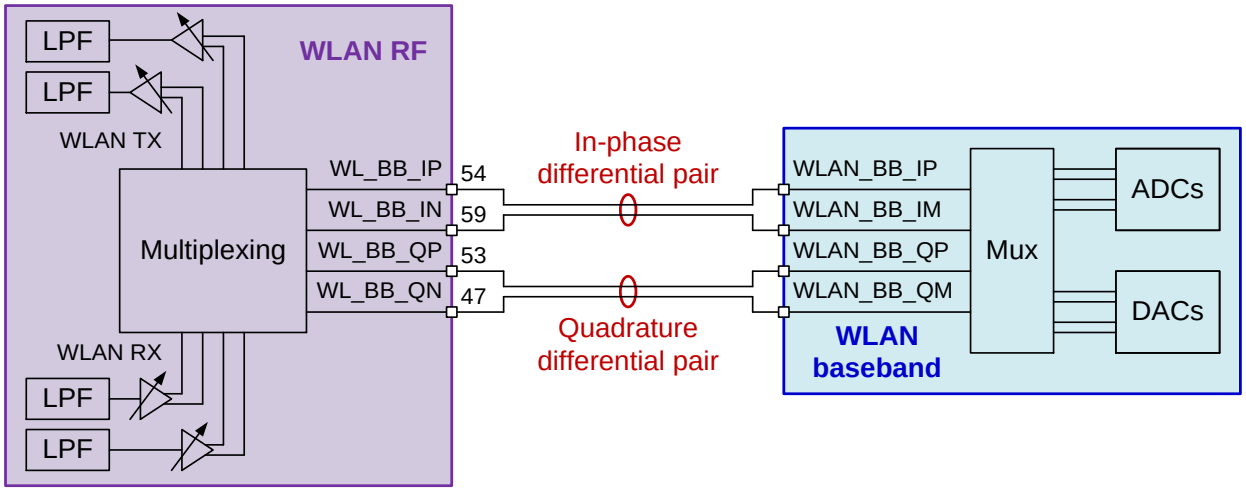

Figure 3-3 WLAN analog baseband interface schematic

3.5 WLAN digital baseband

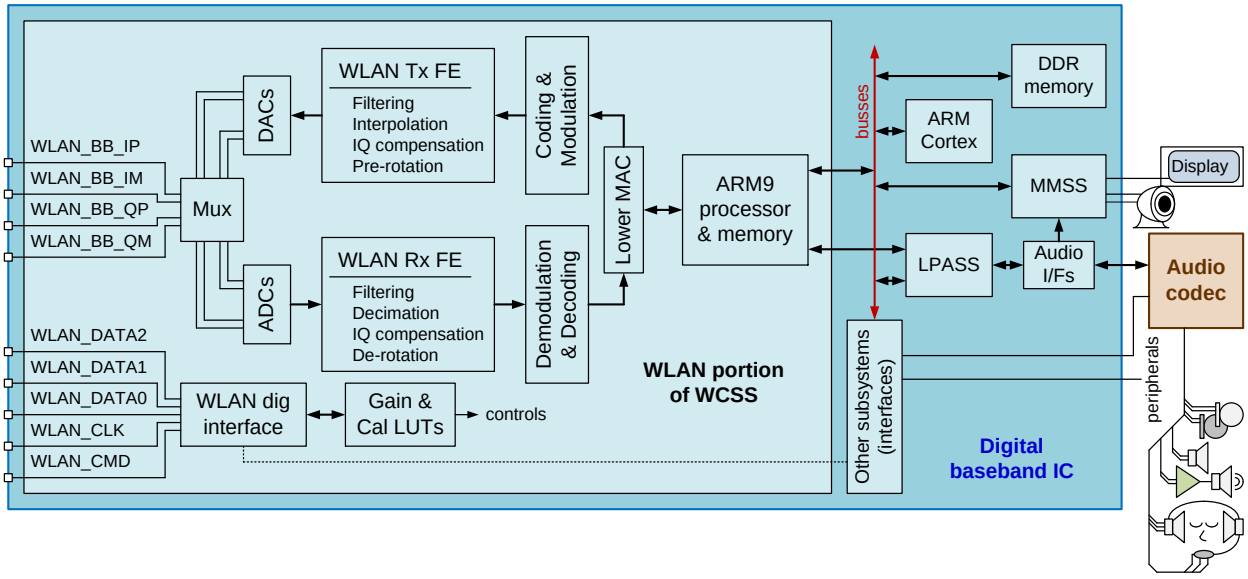

Figure 3-4 WLAN digital baseband

- The WLAN ADC and DAC circuits are integrated into the digital baseband IC.
- The analog baseband interface multiplexes Tx and Rx signals to/from the WCN.
- WLAN uses several digital baseband blocks in addition to the wireless connectivity subsystem (WCSS).
  - Examples: The APQ8016E peripheral subsystem, multimedia subsystem, ARM®Cortex microprocessor subsystem, memory support, and low-power audio subsystem
  - See the appropriate chipset design guidelines for other block details and off-chip I/Os
- This section focuses on the WLAN portion of the WCSS.

- WLAN baseband circuits perform TCP/IP processing and transfer 802.3 frames between other digital baseband subsystems.
- The WLAN digital baseband block converts 802.3 frames into 802.11 frames, performs modulation, and sends analog waveforms to the WCN RF transceiver block for processing and transmission.
- The process is reversed for a received 802.11 frame.

3.6 WLAN modem and ARM processor

ARM926EJ-S → 240 MHz; 32 kB I-cache, 32 kB D-cache.

Memory configuration → 40 kB memory for WLAN internal data structures and BT/FM data; 64 kB ROM is connected directly to the ARM9 I-TCM port.

An upper media access controller (MAC) is driven by software and runs on the embedded ARM.

The lower MAC functions are fully implemented by dedicated circuits (hardware).

Rx mode

- ADCs digitize the analog baseband data from the WCN device.
- Rx front-end hardware performs filtering and decimation, I/Q compensation, and derotation.
- The digital signal is demodulated and decoded by a dedicated hardware block.
- The Rx MAC forwards data to the ARM for upper-layer MAC processing and transfers to the other digital baseband subsystems like multimedia, peripherals, etc.

Tx mode

- The Tx MAC accepts data from the other digital baseband subsystems via the ARM.
- The digital data is encoded and modulated by a dedicated hardware block.
- Tx front-end hardware performs filtering and interpolation, I/Q compensation, and prerotation.
- DACs convert the digital signals to the analog domain and route them to the WCN device.

The internal memory is partitioned into packet memory and data memory.

- Packet –stores both the Rx and Tx frames for the hardware to process.
- Data –contains the data structures with Tx/Rx parameters needed by the hardware modules.

3.7 WLAN digital interface and controller

Five-line proprietary digital interface

- Register read/write and Rx/Tx gain control command with special functions
- Supports 60 MHz for WLAN commands from WCSS to the WCN
- WCN3620 IC master clock selection and enable/disable function

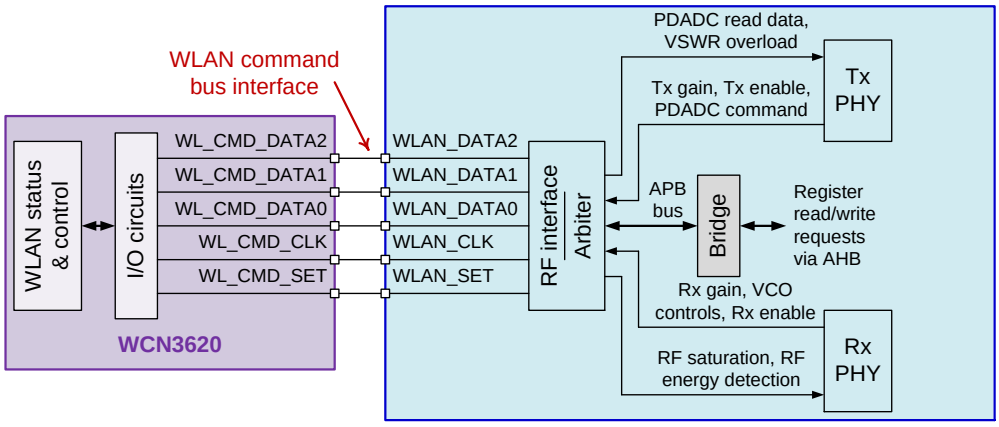

Figure 3-5 WLAN digital interface and controller

Supported functions

- RF mode selection for Tx/Rx
- Tx gain command§ Rx gain command
- Rx antenna shunting§ Auto oscillator calibration
- RF register write
- RF register read
- HKADC control/read command
- RF saturation detection
- RF energy detection
- VSWR overload detection

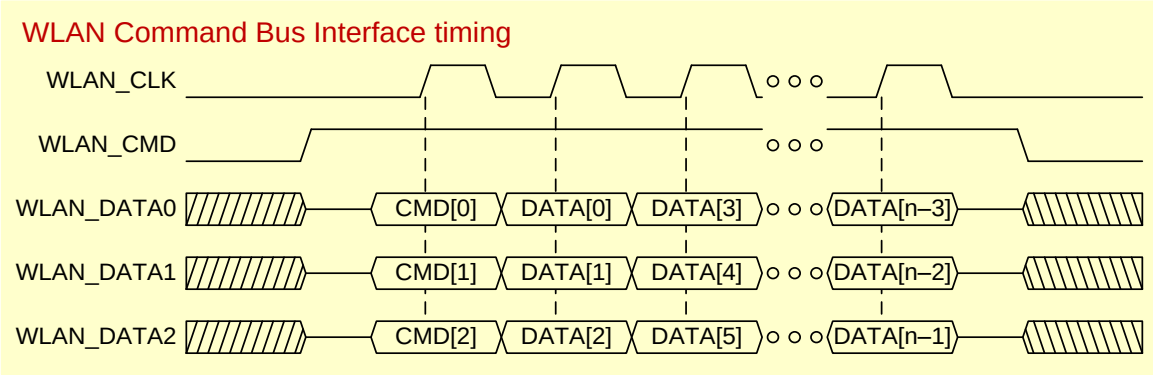

Figure 3-6 WLAN command bus interface timing

3.8 WLAN operating modes

- The application programming interface (API) is used to program WLAN functions.
- The WCN3620 primary operating mode is determined by software. For each valid mode, the appropriate analog, RF, LO, and digital baseband circuits are powered on and unnecessary circuits are turned off.

Table 3-1 WLAN operating modes

Mode	Description
Off	WLAN is off.
Standby	WLAN is configured but not used; WLAN can be enabled quickly from this state. Power supplies are on, but clocks and related circuits are off.
Active	WLAN switches between active and sleep modes for predetermined intervals. When active, beacon packet processing is performed.
Beacon mode power save (BMPS)	WLAN is sleeping, except when the host wakes it up for full-duplex VoIP traffic transmission and reception.
Unscheduled automatic power-save delivery (uAPSD)	All necessary receiver signal paths and LO-related circuits are turned on; the WLAN transmitter is off. Supplies are turned off internally to save power in uAPSD mode.

In addition to controlling the primary operating mode, host software defines the following functions and parameters.

3.8.1 Physical layer parameters

- Transmit power level
- 802.11 data rates
- Modulation type
- Inter-frame spacing
- Rx/Tx chain selection

3.8.2 MAC parameters

- Tx frame size
- Frames-received counter
- Received signal strength indicator (RSSI)

3.8.3 Transceiver-related functions and parameters

- Internal bias conditions; enabling and disabling circuit blocks
- Shared oscillator (Rx/Tx); LO synthesizer circuitry
- Tx power detector
- Baseband parameters and registers
- Test and calibration functions

4 WCN3620 Bluetooth

4.1 Bluetooth high-level comments

The Bluetooth solution is split between two devices: the radio modem (WCN3620 RF transceiver IC) and the controller (the WCSS within the digital baseband IC).

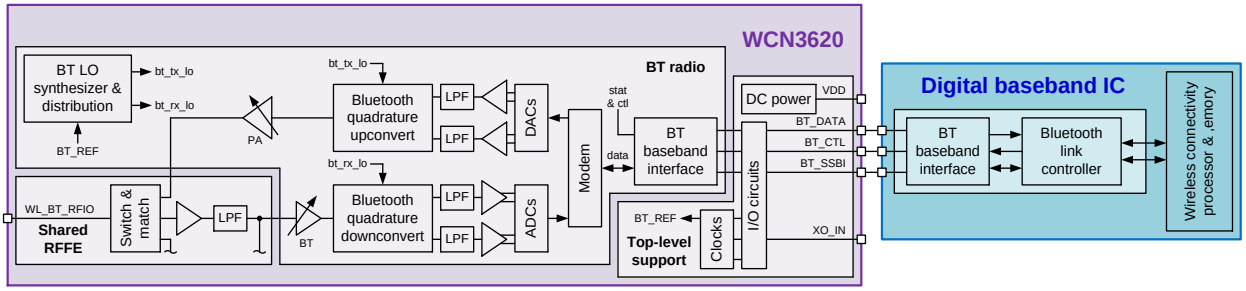

Figure 4-1 Radio modem and controller

This section includes the following Bluetooth information:

- Bluetooth RF transceiver overview
- RF schematic and layout guidelines
- Bluetooth modem
- Interfacing with the digital baseband IC
- Bluetooth digital baseband –overview and details (digital baseband IC functions)
- BR_EDR and LE controllers
- NVM parameters and ROM patches
- Sleep controller and low-power page scan

4.2 Bluetooth RF transceivers

- RF I/O port is shared with 2.4 GHz WLAN
- Integrated switching and matching
- Single-ended RF port

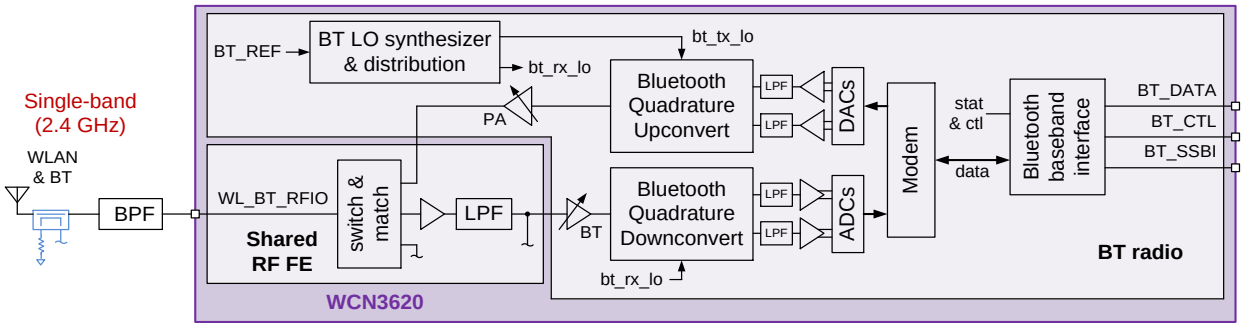

Figure 4-2 Bluetooth RF transceivers

4.3 Bluetooth digital data interface with the digital baseband IC

Two-line proprietary digital interface

- Serializes control and data
- Return-to-zero (RZ) signaling
- BT_CTL is unidirectional (digital baseband IC master).
- BT_DATA is bidirectional.
  - Direction is set by Rx/Tx slot type
- Pins are tri-state when the link is idle

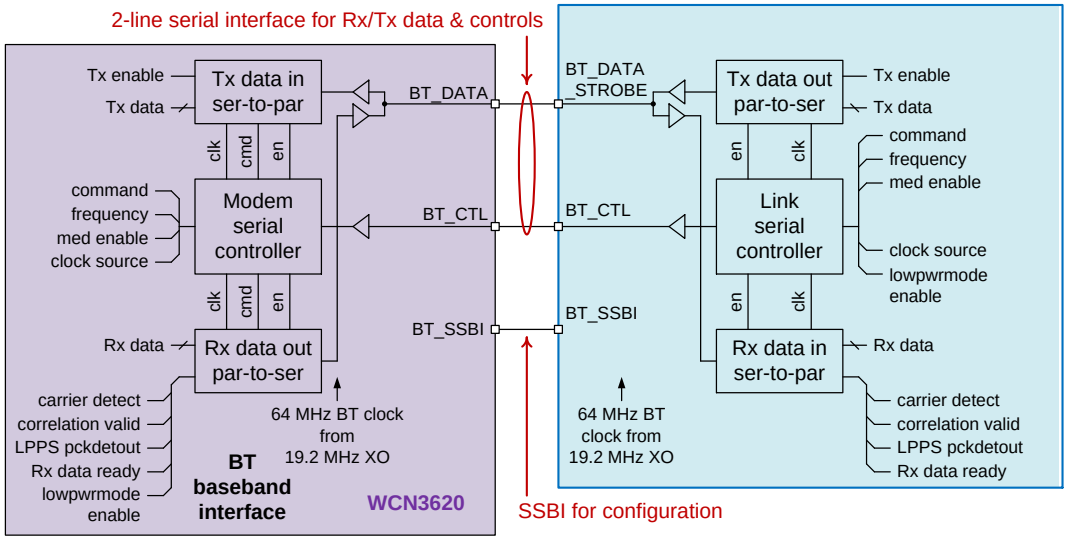

Figure 4-3 Bluetooth digital data interface with the digital baseband IC

4.4 Bluetooth operating modes and coexistence

The application programming interface is used to program Bluetooth (BT) functions.

The primary Bluetooth operating mode is determined by handset software. For each valid mode, the appropriate circuits are powered on and configured properly while circuits not required are powered off.

In addition to these primary operating modes, key BT circuit characteristics are configurable.

- Bluetooth features and device address
- RF control parameters including Tx power amplifier (PA) gain and power control
- Sleep mode enable/disable and sleep parameters

Table 4-1 Bluetooth operating modes and coexistence

Mode	Description
Off	All power supply sources are shut down internally and all circuits are off. To exit the off state, the full initialization and configuration process must be executed.
Sleep	The main processor, RF and analog circuits, and select power supplies are shut down during periods of inactivity. Exiting the sleep state restores operating parameters so that active operation can resume immediately without host intervention.
Active	Needed power sources are connected internally, needed circuits are enabled, and Bluetooth operates normally (page scan, inquiry scan, ACL connection, data transfer, SCO/eSCO connection, etc.).

See Section 3 WCN3620 Wireless Local Area Network for coexistence information.

4.5 BR_EDR and LE controllers – parallel implementations

Features for the LE controller are implemented in parallel with the BR/EDR controller.

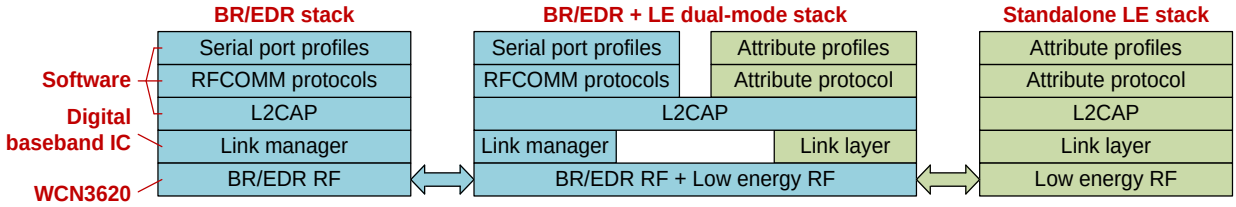

Figure 4-4 Parallel implementation of LE controller with BR/EDR controllers

4.6 NVM parameters and ROM patches

All Bluetooth/FM/WLAN code is read and executed from the system DDR memory.

The applications processor is responsible for downloading WCSS software from flash to DDR memory and for performance optimization.

- Several Bluetooth NVM parameters are configurable, thereby allowing functional customization and performance optimization.
- Bluetooth WCSS software configures the hardware functions based upon the default values built into the WCSS image for these parameters.
- Host software running on the applications processor has the capability to override the default parameters.

- Changes require an internal reset command that forces the hardware to read and implement the new RAM values, thereby overriding any previously loaded configuration parameters.

All configuration overrides are lost upon power loss or hardware reset. The host must reload all configuration parameters.

4.7 Sleep controller

The Bluetooth (BT) block allows low-power operation to minimize current consumption. Sleep is one of the low-power states, characterized by no BT RF activity, no master reference clock use, and no processor activity, and resulting in low current consumption.

During sleep, the BT block shuts down all processors and most power supplies, and the master reference clock is disabled; BT circuits operate off the sleep clock (or low-power oscillator [LPO]).

Sleep-mode entry cannot be forced; it can only be entered by a voting algorithm in which several criteria must be satisfied before sleep occurs. All of the following criteria must be satisfied to enter sleep mode:

- Sleep is enabled by configuration.
- All communication with the host is complete, with none pending.
- No radio traffic is scheduled for at least one frame.
- No SCO or eSCO connection exists.
- The ARM9 processor is not processing data.
- The LPO is available.
- Wake is not commanded by the host.

Waking from sleep is triggered by one of two sources:

- The BT block is automatically awakened by internal timer expiration to process scheduled air traffic, such as page scans and sniff slots.
- The host is also able to wake the BT block.

4.8 Low-power page scan

When sleep mode is enabled, the BT block has two page-scan options: normal page scan and low-power page scan. Relative to the normal page scan, the low-power page scan (LPPS) reduces current consumption by about 40%.

Both the sleep mode and the LPPS mode are enabled in NVM. The procedure is:

- Software opens a 11.25 ms scan window and looks for energy within the scan window.
- LPPS is exited on the first energy-detect interrupt.
- Software then schedules a normal scan.

5 WCN3620 FM Radio

5.1 FM radio high-level comments

The FM radio solution is split between two devices: the radio modem (WCN3620 RF transceiver IC) and the controller (the WCSS within the digital baseband IC).

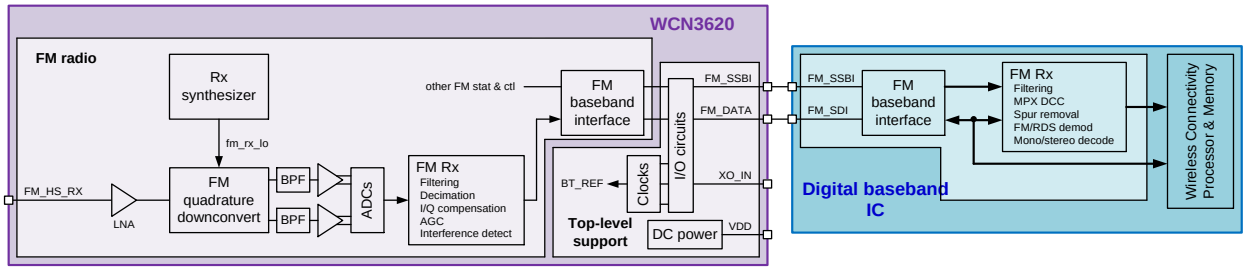

Figure 5-1 Radio modem and controller

This section includes the following WLAN information:

- FM RF receiver overview
- FM RFIOs and Rx port tuning
- RF schematic and layout guidelines
- Digital interface with the digital baseband IC
- FM radio operating modes
- FM digital baseband –overview and details (digital baseband IC functions)

5.2 FM RF transceivers

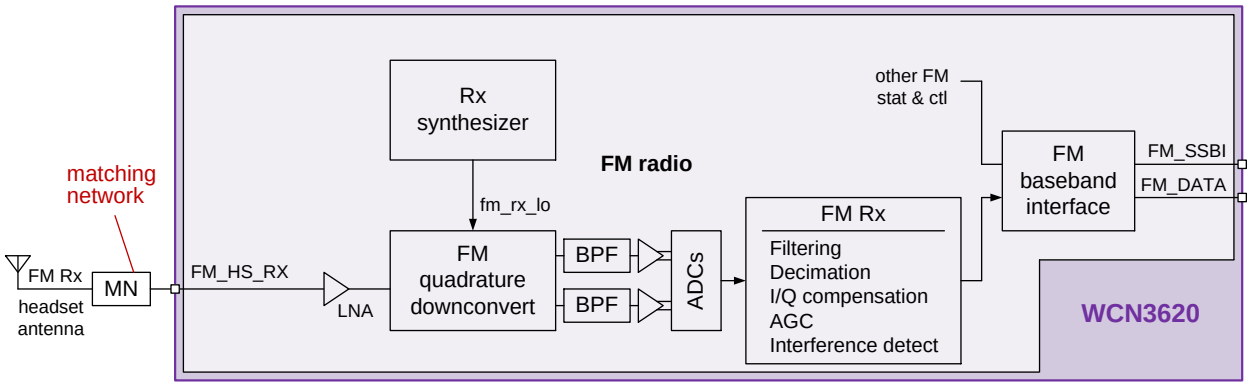

Figure 5-2 FM RF transceivers

- One RFIO ports supports one antenna configuration.
  - Headset cable ground antenna for Rx-only
- Single-ended RF port
- Simple two-line interface with the digital baseband IC

5.3 FM RF details – layout guidelines

Comments within the WLAN and Bluetooth RF layout figures apply for FM as well

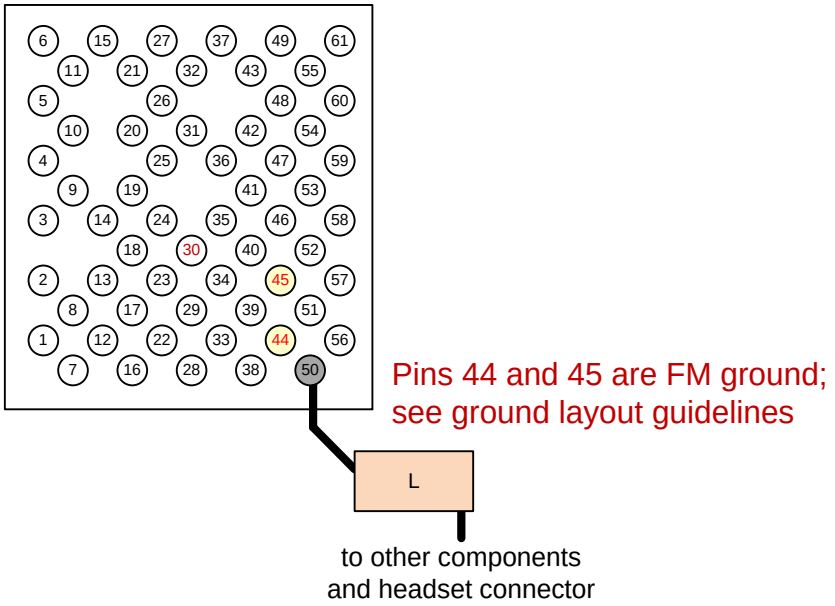

Figure 5-3 FM RF details layout guidelines

5.4 FM radio digital interface with the digital baseband IC

Rx mode runs at 9.6 MHz.

- Samples at 240 kHz
- 16 in-phase bits + 4 zero bits
- 16 quadrature bits + 4 zero bits
- 0.24 × 40 = 9.6 MHz

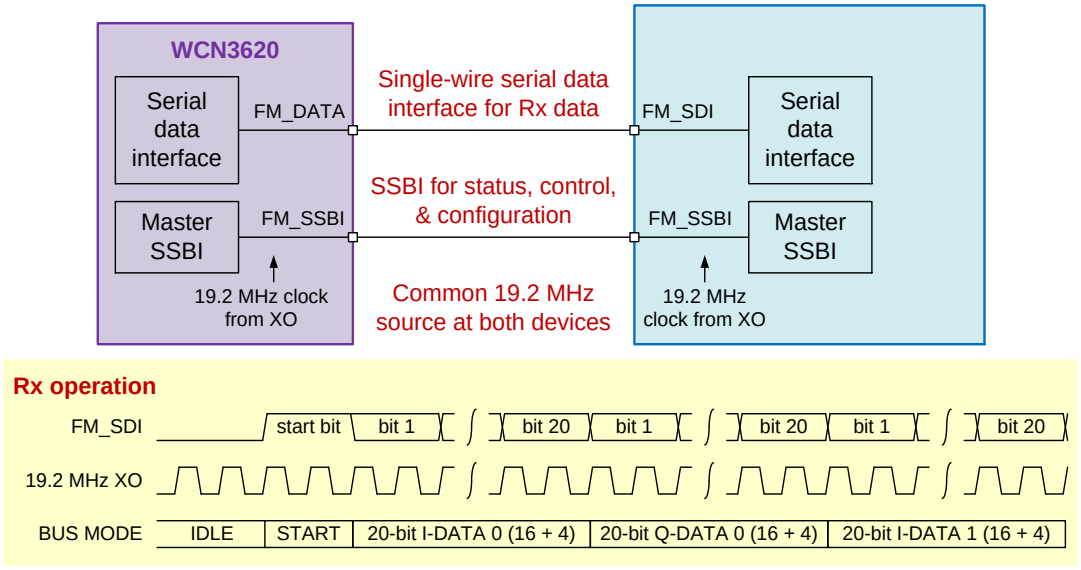

Figure 5-4 FM radio digital interface with the digital baseband IC

5.5 FM radio operating modes

The API is used to program FM radio functions.

The primary FM radio operating mode is determined by handset software. For each valid mode, the appropriate circuits are powered on and configured properly while circuits not required are powered off.

In addition to these primary operating modes, key FM circuit characteristics are configured as needed.

Table 5-1 FM radio operating modes

Mode	Description
Powerdown	All power supply sources are shut down internally and all circuits are off. To exit the off state, the full initialization and configuration process must be executed.
Receiver on	Needed power sources are connected internally, needed circuits are enabled. Rx operation occurs simultaneously with a phone connection.
Transmitter	Tx mode is NOT supported.

5.6 FM radio digital baseband

The FM radio interfaces to/from the WCN device (SDI for Rx data; SSBI for status, control, and configuration) were discussed earlier in this section.

FM uses several digital baseband IC blocks in addition to the WCSS.

- Examples include the peripheral subsystem, multimedia subsystem, ARM cortex microprocessor subsystem, memory support, and low-power audio subsystem (depending upon the digital baseband IC).

- See the appropriate chipset design guidelines document for details about these other blocks and off-chip I/Os.

This page focuses upon the FM radio portion of the WCSS.

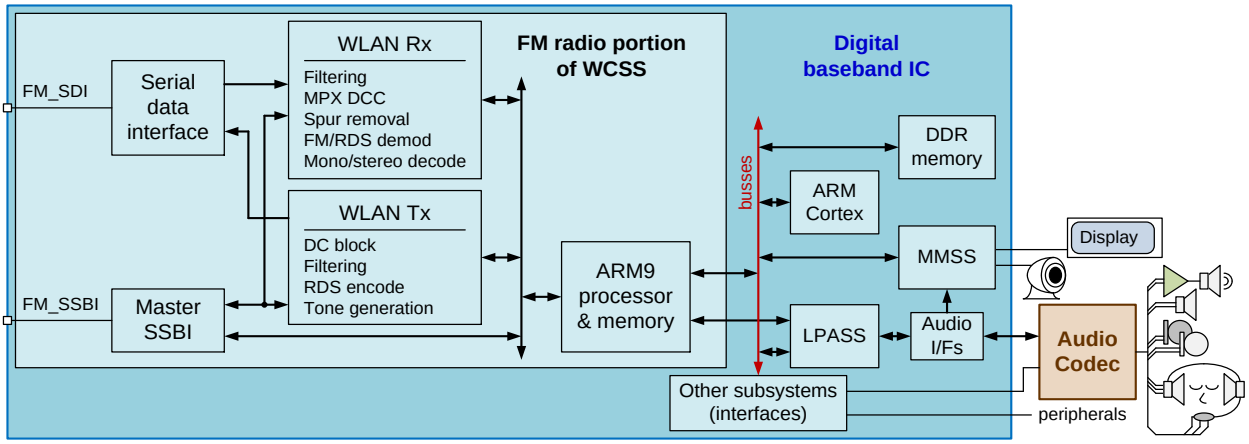

Figure 5-5 FM radio digital baseband

ARM9 material (and beyond) is discussed in Section 3 WCN3620 Wireless Local Area Network.

Clock distribution details are presented in Section 6 WCN3620 Shared Support Functions.

6 WCN3620 Shared Support Functions

6.1 WCN shared top-level support – high-level comments

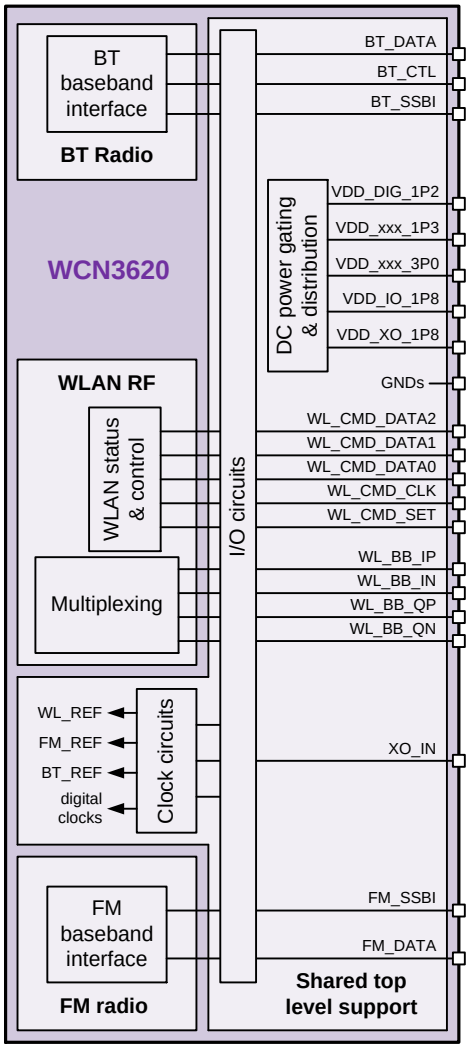

Figure 6-1 WCN3620

Some WCN functions are shared by the three main circuit blocks (WLAN, BT, FM radio) –these shared functions are examined in this section.

- The I/O circuits that interface with the digital baseband IC –and configure the WCN for the desired operation
- System clock options –external XO 19.2 MHz from PMIC
- Clock details – buffering, gating, and distribution to other internal blocks; layout guidelines for the crystal implementation
- The support block manages all WLAN, BT, and FM interfaces with the digital baseband IC
- DC power supply gating and distribution to other internal blocks –including power sequencing

6.2 WCN shared top-level support – I/O circuits

- The three digital interfaces for the subsystems – WLAN, Bluetooth, and FM radio are processed by the top-level mode multiplexer (TLMM).

- The clock signal and the WLAN analog baseband signals are simply passed through the I/O circuit block.
- Each subsystem has its own interface circuits, registers, and bus.
- The WLAN registers are also used for top-level functions.

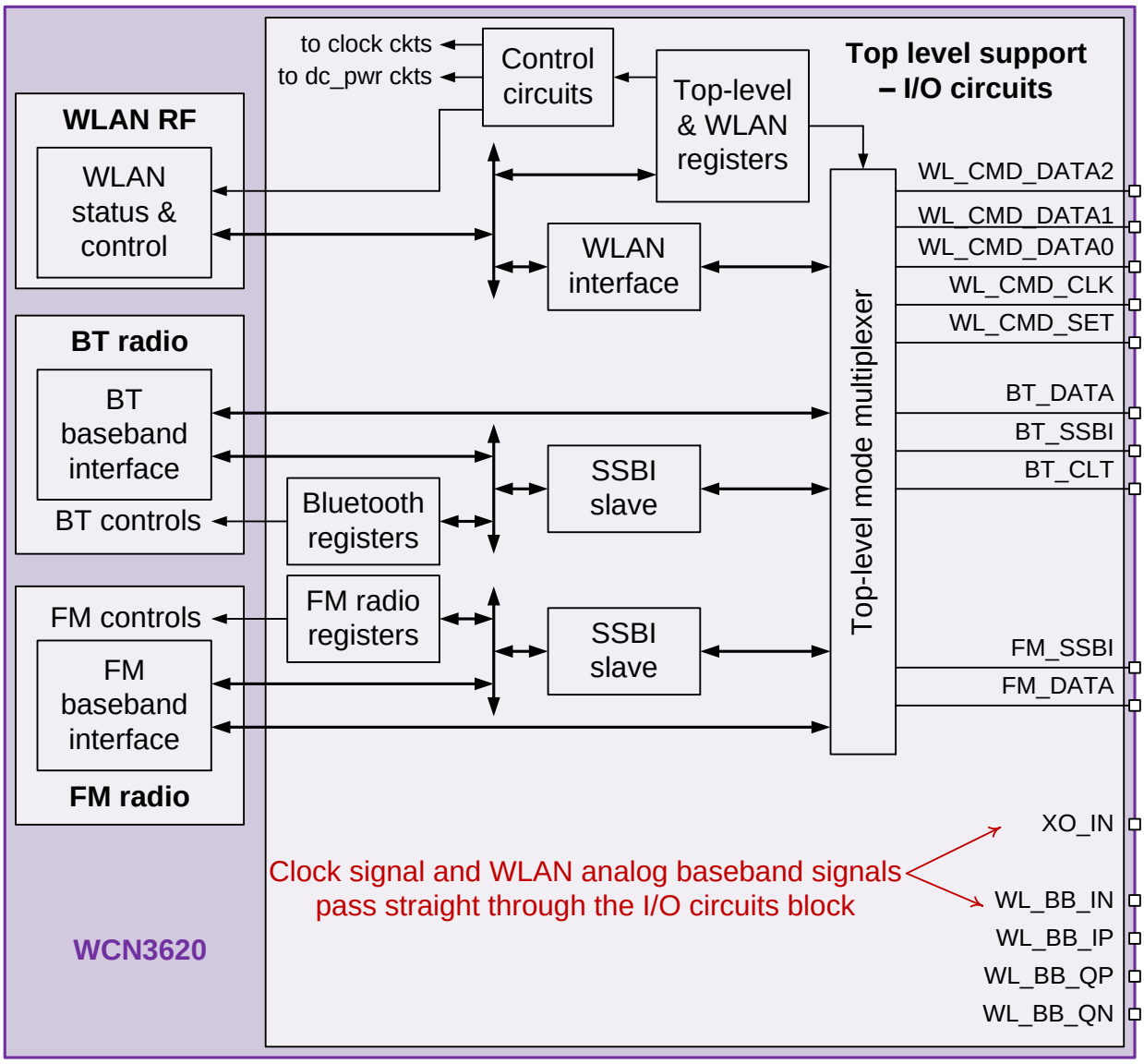

Figure 6-2 WCN I/O circuits

6.3 Configuring the WCN3620

Each WCN3620 block requires configuration.

- The shared top-level support block is configured via the WLAN five-line interface; parameters to be configured include:
  - Pull status and direction for digital pads in test or debug modes

- Clock details
- WLAN is configured via its five-line interface
- Bluetooth is configured via its dedicated SSBI; parameters to be configured include:
  - BT address –must be unique for each device
  - Master reference clock frequency
  - ROM patches
  - Sleep control, power configuration, etc.
- FM radio is configured via its dedicated SSBI; parameters to be configured include:
  - FM address
  - DAC configuration
  - FM digital configuration

After loading NVM configuration parameters, the host must send the reset command for the new configurations to be activated.

Also see Section 4.6 NVM parameters and ROM patches.

6.4 WCN shared top-level support – clocks

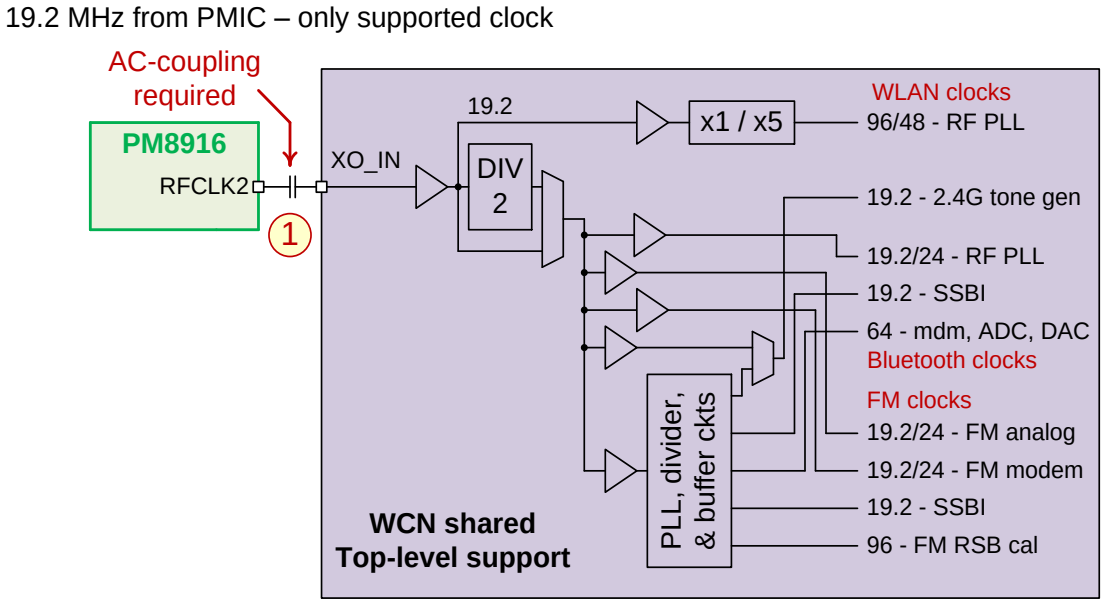

Figure 6-3 WCN clocks

See appropriate chipset-level design guidelines for overall clock distribution details – from PMIC to all other ICs

6.5 DC power and WLAN_BT_FM power domains

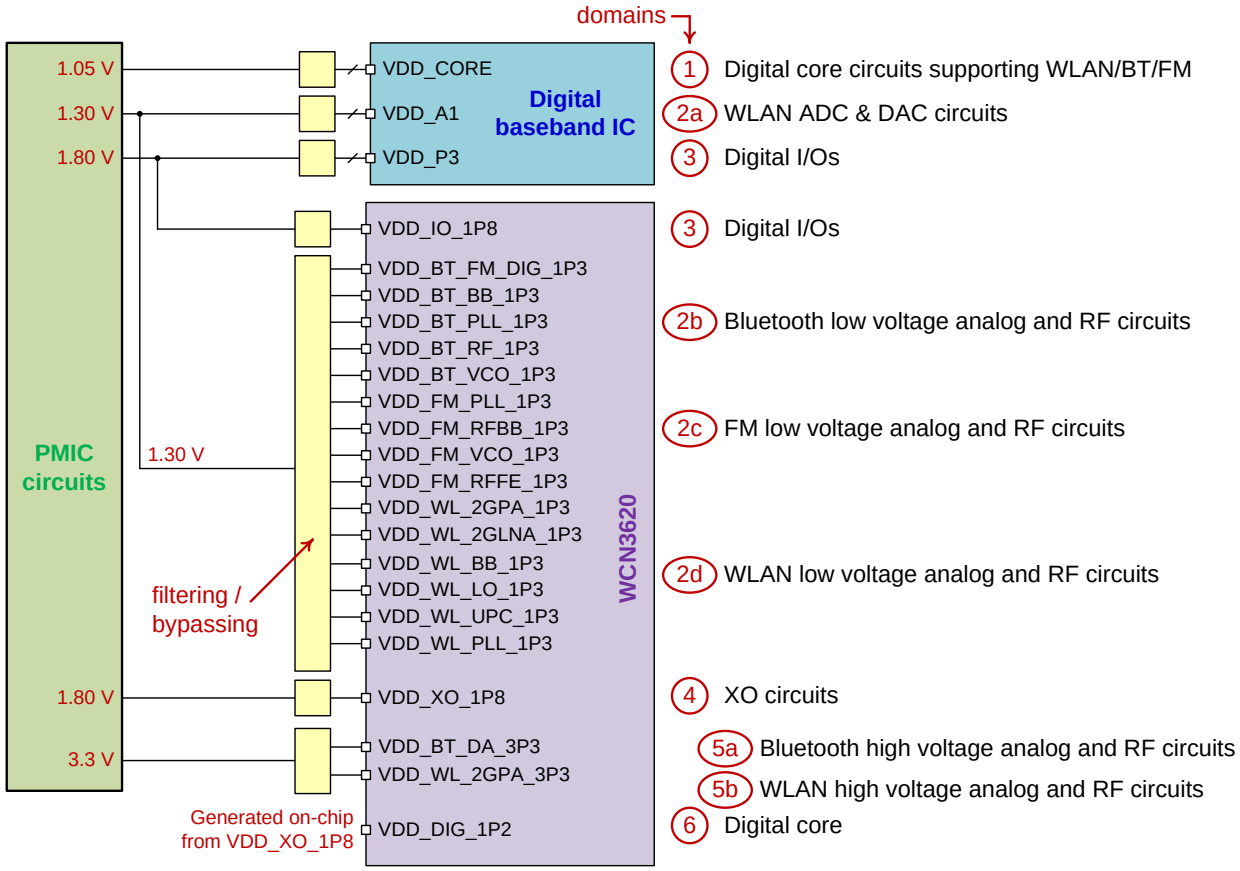

Figure 6-4 DC power and WLAN_BT_FM power domains

6.6 Power-sequencing and power-saving techniques

6.6.1 Power-saving techniques

- Clock gating (static and dynamic)
- Use flop trays
- Static clock frequency scaling based upon the bandwidth mode (20/40/80 MHz bandwidth)
  - Group A –60/120/240 MHz clock
  - Group B –80/160/320 MHz clock
  - Group C –30/60/120 MHz clock
- Dynamic frequency scaling
  - Internal engines scale the clocks based upon the packet Tx or Rx rate.
- Clocks to unused modules are switched off in certain power saving modes.

- Multiple GDHS domains
- SPM supports RPM handshaking.
- Power saving modes
  - WLAN unscheduled APSD
  - WoWL power-save mode
  - WLAN beacon power save-related sleep
  - WLAN standby
  - WLAN deep sleep (inactive)
  - Bluetooth sleep
  - Bluetooth inactive
  - FM inactive

6.6.2 Power sequencing

Poweron: Below is the proper poweron sequence to reduce leakage current. Allow at least 200 μs for LDO settling:

1. 1.8 V XO, 1.8 V IO (either 1.8 V can turn on first)
2. 1.3 V
3. 3.3 V

Powerdown: Below is the proper powerdown sequence to reduce leakage current:

1. 3.3 V and 1.3 V simultaneously
2. 1.8 V XO, 1.8 V IO (either 1.8 V can turn off last)

7 Digital Baseband IC Wireless Connectivity Support

7.1 Digital BB IC wireless connectivity architecture and topic overview

A high-level diagram of the digital baseband IC wireless connectivity and supporting functions is shown in Figure 7-1.

① Each wireless technology has dedicated interfaces with the digital IC; topics covered:

- WLAN
  - Secure digital for status and control and analog baseband for Rx and Tx data
- BT
  - 2-wire serial bus for data and SSBI for status and control
- FM radio
  - 1-wire serial data interface for data and SSBI for status and control

② Most audio functions are within the WCSS; details are presented about:

- Architecture, buses, and clocks

③ Audio is supported using an audio codec such as the WCD9302 or WCD9306, the digital baseband IC's WCSS, and other digital IC functions, including:

- Low power audio subsystem (LPASS)
- WCD interfaces –SLIM bus and discrete status and control lines
- Other support functions like a microprocessor subsystem, peripheral subsystems, etc.

④ Integrated WCSS/LPASS interfaces improve overall efficiency

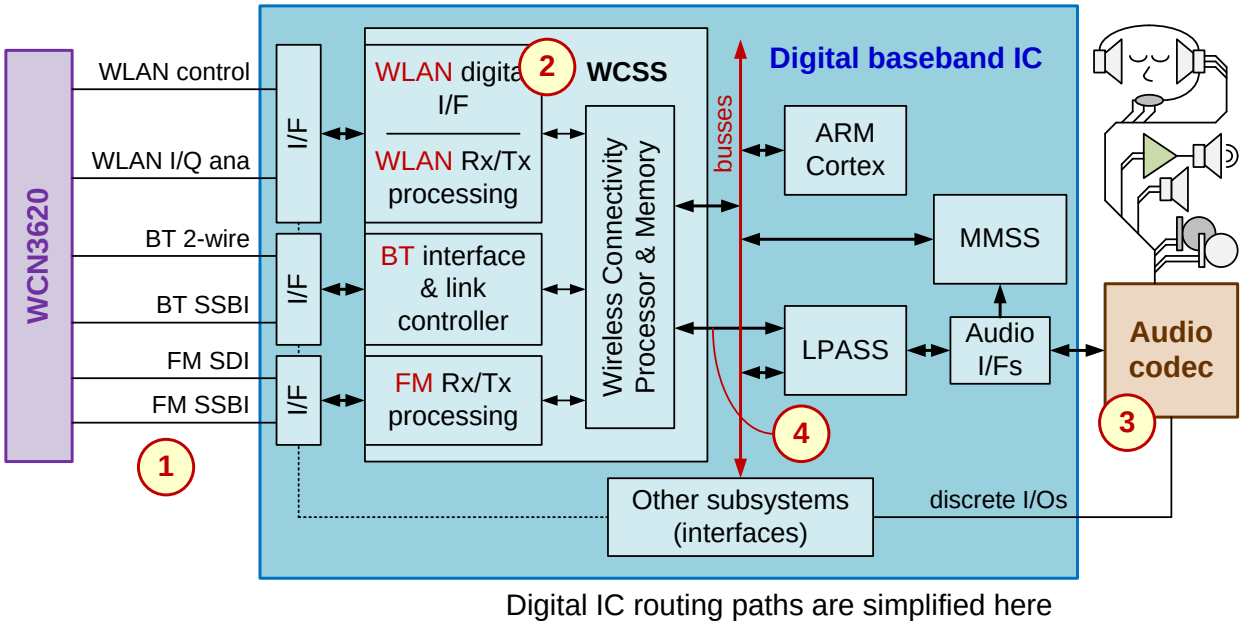

Figure 7-1 Digital BB IC wireless connectivity architecture

7.2 Digital baseband IC wireless connectivity subsystem

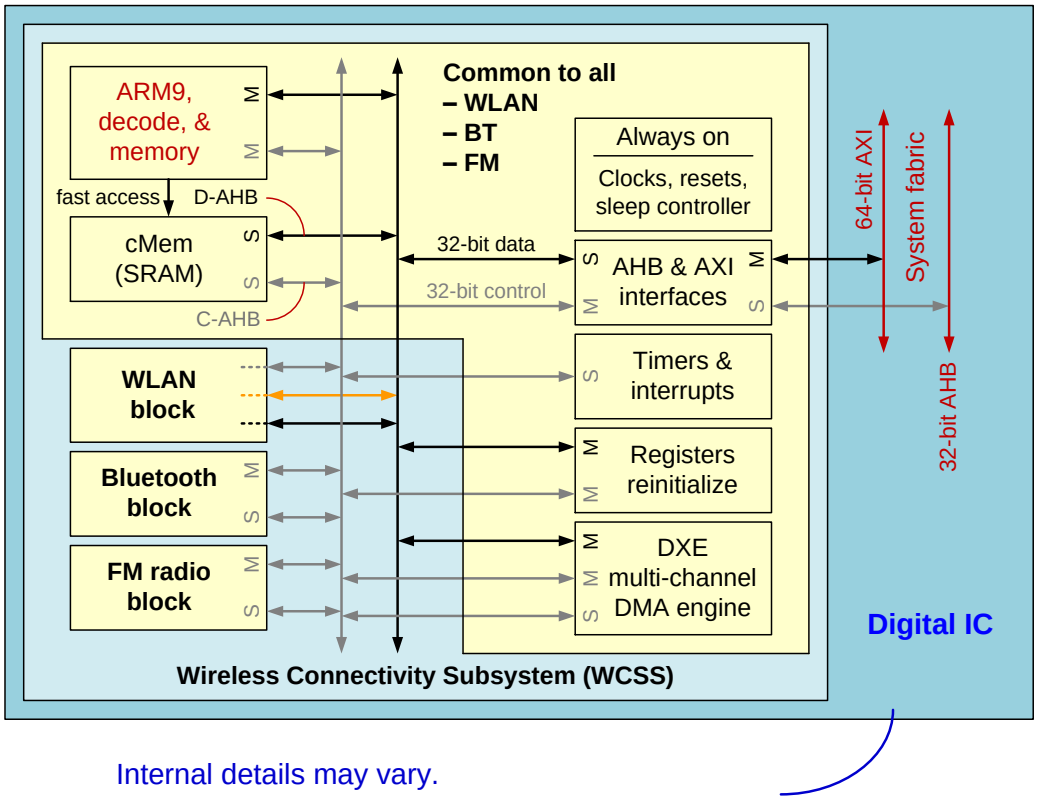

Figure 7-2 Digital baseband IC wireless connectivity subsystem

Overall WCSS architecture was shown on the previous page.

Additional details are presented within other sections, organized by functionality (see the "WLAN analog baseband interface – schematic," "Bluetooth digital data interface with the digital baseband IC," and "Bluetooth digital data interface with the digital baseband IC" pages).

Major WCSS functions are:

- WLAN block
- Bluetooth block
- FM radio block
- A common block shared by all three that includes:
  - ARM926EJ-S and its memory
    - 240 MHz; 32 kB I-Cache; 32 kB D-Cache; I-TCM port connected to ROM
    - 40 kB memory used for internal data structures and BT/FM data; 64 kB ROM connected directly to ARM9 I-TCM port
  - DXE multichannel DMA engine
  - Two AHB buses
    - D-AHB for data transfer between the WLAN block, SRAM, and system fabric
    - C-AHB for control flow within WCSS and external modules and packet flow for Bluetooth and FM radio
  - This common block provides interfacing between WLAN, Bluetooth, and FM blocks and the system fabric.
  - Its architecture provides efficient interfaces while minimizing transactions to the system fabric.

7.3 WCSS internal bus interfaces

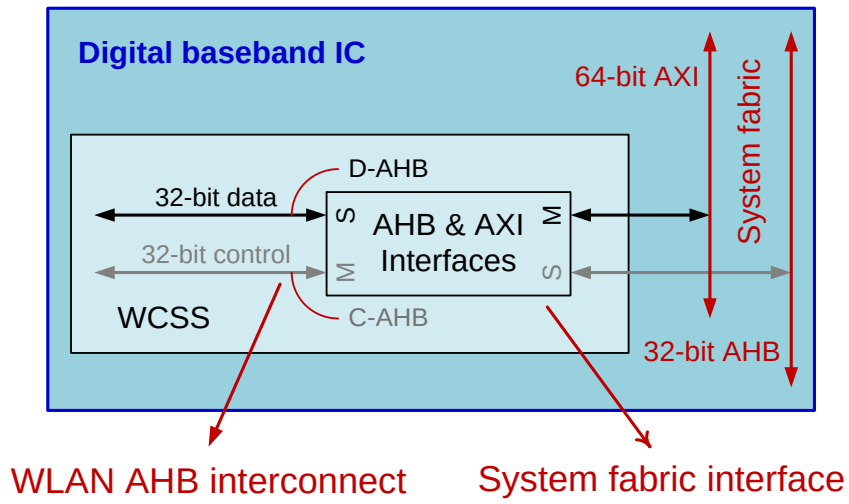

Figure 7-3 WCSS internal bus interfaces

7.3.1 WLAN AHB interconnect

- 32 bits wide
- Standard AHB bus IP from Synopsys Designware IIP library
- Builds on basic AHB bus protocol: standard bus monitors and protocol checkers still usable
- Adds sidebands to standard signals
  - Byte strobes
    - Permit efficient single-burst unaligned transfers
    - Eliminate multiple arbitration latency penalties
  - Transfer length
    - Any length from 1 to 128 bytes in a single transfer; increases bus efficiency and minimizes arbitration and access latencies
    - Exact length communicated to slave provides efficient pre-fetching of data – no wasted bus bandwidth
  - Sideband additions map well to AXI protocol support for byte strobes and exact length transfers – easier coding of WLAN AHB to AXI slave
- Support for split transfers avoids hanging the bus until previous request is completed and allows immediate forwarding of new request to destination slave

7.3.2 System fabric interface

AHB lite port

- Connects System Fabric to internal control bus via A2AB bridge
- No support for Early Burst termination
  - All efficient multimaster AHB busses generate EBTs under various common scenarios; requires AHB bus bridge to connect to fabric
- No support for splits
  - Bus hangs for long periods due to fabric arbitration and latencies
  - Other masters cannot use bus even to interface with a slave
  - Precludes forwarding new request
- 32-bit max width so maximum possible burst size is 64 bytes
  - Less efficient; full arbitration and memory latencies each burst AXI port
- Best option for data bus
- 64-bit width allows 128 byte burst sizes (16 beat bursts × 64-bit)
- Protocol support for byte strobes and exact transfer lengths provides more efficient transfers
- Requires AHB to AXI bridge for protocol conversion (A2XB)

7.4 Data AHB bus (D-AHB)

Provides data transfers between the system fabric, the common block, and the WLAN block.

Using D_AHB:

- DXE transfers BT and FM data between the digital IC's DDR memory and cMEMSRAMs.
- DXE transfers WLAN packets between the digital IC's DDR memory and the WLAN block.
- WLAN sub-modules also access the data structures in cMEMSRAMs.
- WCS accesses the digital IC's DDR memory through D_AHB only.

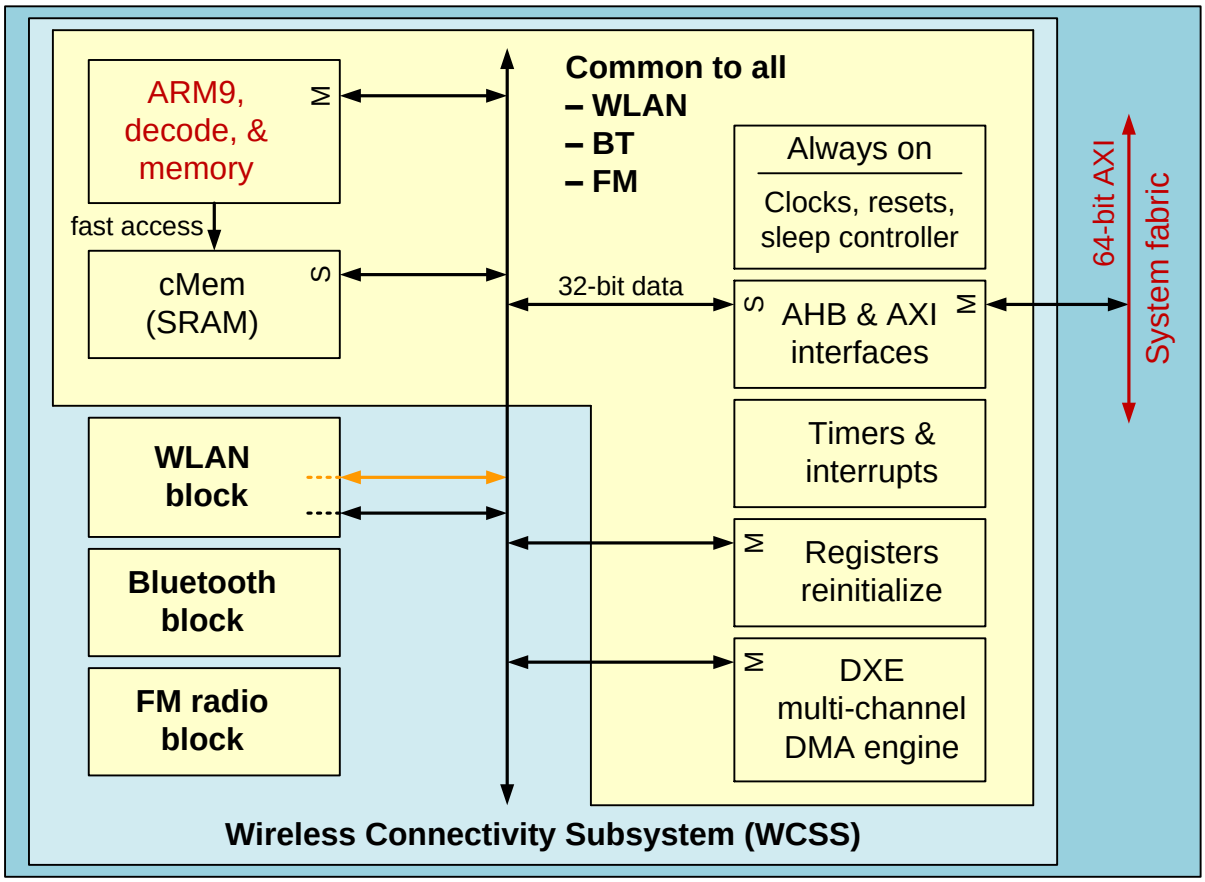

Figure 7-4 Data AHB bus

7.5 Control AHB bus (C-AHB)

Provides control access to every module in the common block and the other WCSS blocks.

- Three AHB masters within the common block are connected through GAM interfaces in the ARM9 + memory address decoder, DXE, and register/re-initialize circuits.
- Three AHB slaves are connected to GAS interfaces in cMEM, DXE, and timers/interrupts circuits.

- Other subsystems and external modules communicate with the WCSS through the C_AHB only.
- All control flow happens on the control bus and is not influenced by any DDR access latencies.

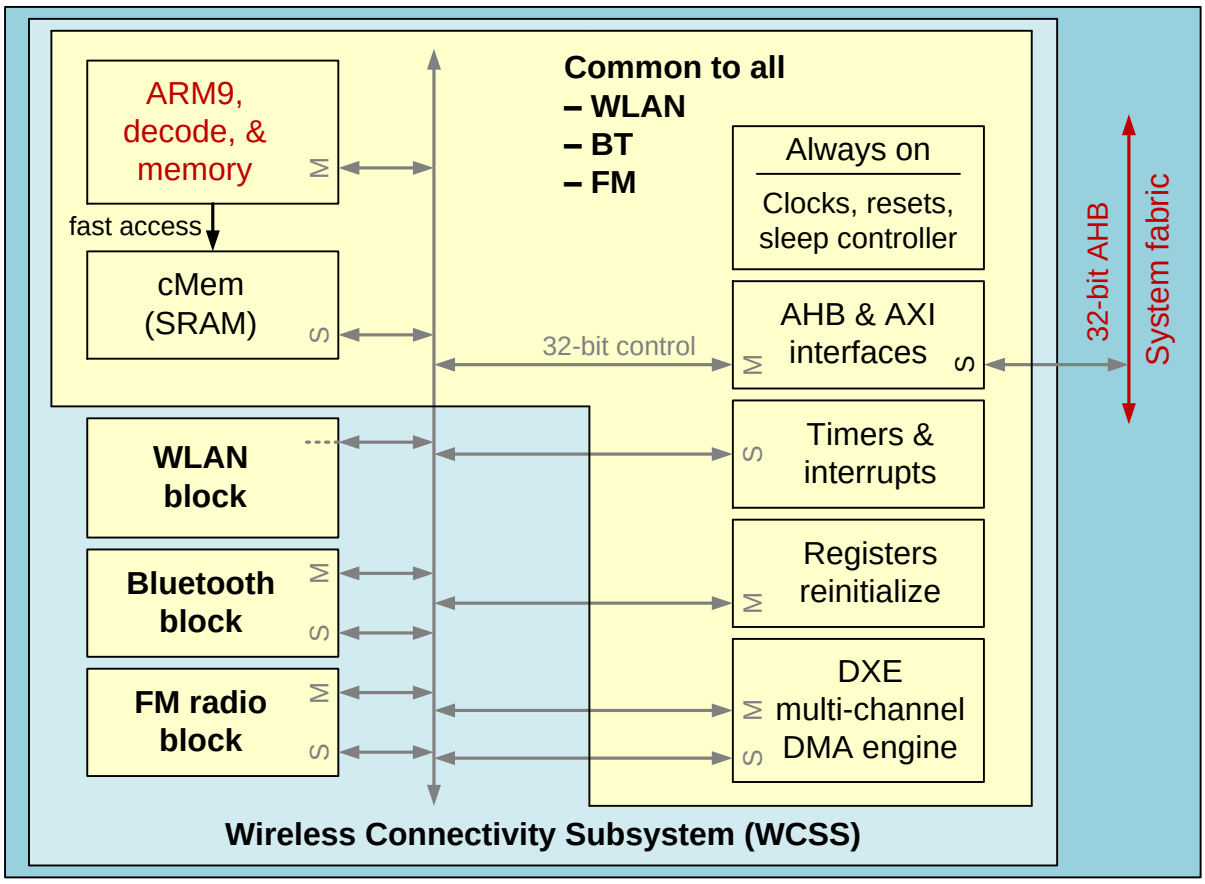

Figure 7-5 Control AHB bus

7.6 WCSS clocks

- The digital baseband IC generates several clocks for WLAN, Bluetooth, and FM radio functions
- The WCSS includes a clock controller that uses these clock sources to generate the needed clocks for:
  - ARM9 and buses
  - JTAG for ARM9
  - ADC and DAC sampling clocks
  - WLAN physical layer core
- Other internal clocks operate from 30 to 320 MHz

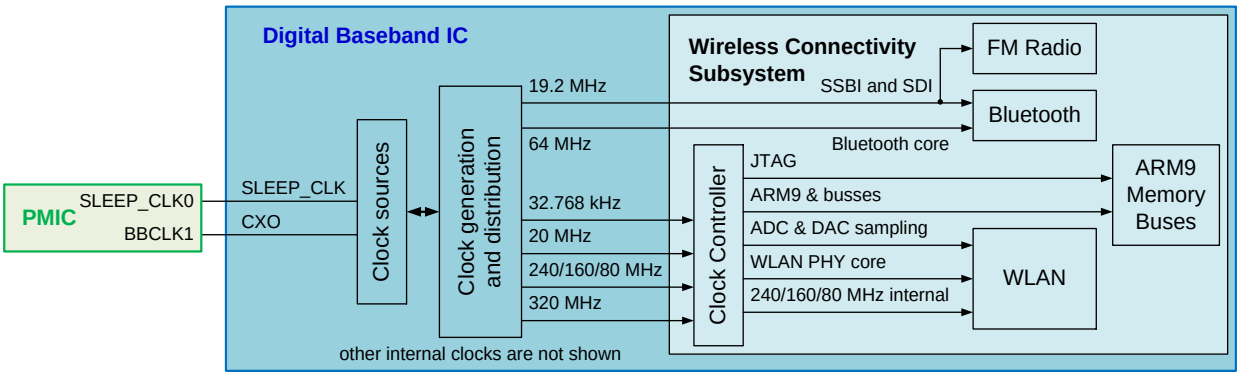

Figure 7-6 WCSS clocks

7.7 Audio support for wireless connectivity – overview

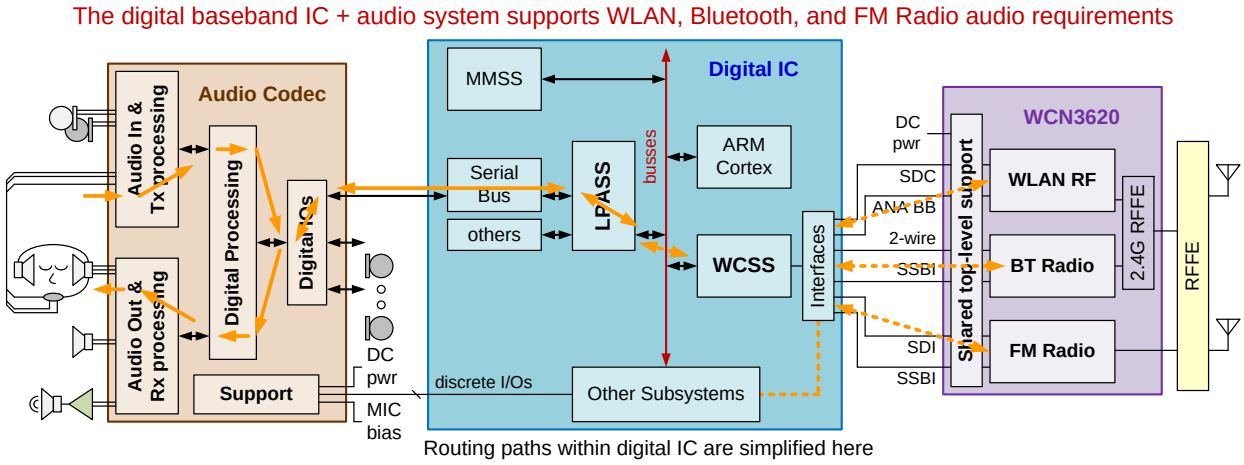

Figure 7-7 Signal flow

7.7.1 General Tx signal flow

- From microphone to Codec audio inputs
- Through digital processing to Codec digital I/Os LPASS
- LPASS to WCSS (or other subsystems for interfaces)
- Through appropriate digital IC / WCN interface
  - WCSS analog baseband for WLAN
  - 2-wire serial interface for Bluetooth
  - SDI for FM Radio

7.7.2 General Rx signal flow

- Through appropriate WCN / digital IC interface – WCSS analog baseband for WLAN – 2-wire serial interface for Bluetooth – SDI for FM Radio
- WCSS (or other subsystems for interfaces) to LPASS
- LPASS
- WCD and through its digital processing
- From WCD audio outputs to speaker(s)

7.8 Audio support for WLAN, Bluetooth, and FM radio

See audio slides or chipset design guidelines for audio content, including:

- WLAN, Bluetooth, and FM radio audio support
- Integrated LPASS and WCSS interfaces
- LPASS and WCSS flow control and interrupts

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