WGR7640 IC GNSS RF Receiver Design Guidelines

September 2016
## Revision history

<table>
<thead>
<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
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<tbody>
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<td>Initial release</td>
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1 Overview

1.1 Purpose

This document provides a description of the WGR7640 IC chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE: Enabling some features may require additional licensing fees.

1.2 Acronyms, abbreviations, and terms

Table 1-1 provides definitions for the acronyms, abbreviations, and terms used in this document.

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
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<tbody>
<tr>
<td>APQ</td>
<td>Application Processor Qualcomm</td>
</tr>
<tr>
<td>CSP</td>
<td>Control Switching Point</td>
</tr>
<tr>
<td>GLONASS</td>
<td>Global NAVigation Satellite System</td>
</tr>
<tr>
<td>GNSS</td>
<td>Global Navigation Satellite System</td>
</tr>
<tr>
<td>GPS</td>
<td>Global Positioning System</td>
</tr>
<tr>
<td>LO</td>
<td>Local Oscillator</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-locked Loop</td>
</tr>
<tr>
<td>PMIC</td>
<td>Power Management Integrated Circuit</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>SSBI</td>
<td>Signal-Signal Beating Interference</td>
</tr>
<tr>
<td>WGR</td>
<td>WLP GPS Receiver</td>
</tr>
<tr>
<td>WLP</td>
<td>Wafer-level Package</td>
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</table>
1.3 WGR7640 within the APQ chipset

Figure 1-1 WGR7640 within the APQ chipset

1.4 Overview of WGR7640 topics

This document provides an introduction to the WGR system, followed by three major sections: RF receivers, baseband interface, and support circuits (as shown in Figure 1-2).

Figure 1-2 WGR7640 top-level layout guidelines
1.5 WGR7640 features

Salient features:

- Small package: 2.07 mm × 1.51 mm × 0.63 mm
- 65 nm wafer-level package (WLP)
- 17-pin CSP
- GNSS stand alone RF receiver
- Compatible with Callisto (Gen8A) GPS digital baseband engine
- Fully integrated synthesizer PLL, VCO, and loop filter components
- Power reduction features for low-power consumption
- Single-line serial bus interface (SSBI)
- The chipset solution includes the APQ + WGR7640 ICs
2 WGR7640 System

2.1 GNSS receiver system block diagram

Dedicated synthesizer used for GNSS operation; provides the LO for the GNSS receiver

WGR7640 IC can be placed close to the GNSS antenna and does not need a GNSS ELNA

I and Q components from the WGR7640 IC are routed to on-chip ADC circuits in the APQ IC, that digitize the received signals and route the serial data streams to the Gen8A Engine.

Figure 2-1 GNSS receiver system block diagram
3 WGR IC Details – RF

3.1 WGR RF receivers high-level comments

- Receiver is implemented in 65 nm RFCMOS process which accommodates high-frequency, high-precision analog circuits and low-power CMOS functions
- Independent receive path from RF to baseband (I/Q)
- Optimized for standalone operation
- Consists of differential RF inputs supporting primary GPS, GLONASS, Compass, Galileo, and QZSS navigation satellite systems. Supported frequency bands are shown in Table 3-1.

Table 3-1 Supported frequency bands

<table>
<thead>
<tr>
<th>Satellite system</th>
<th>Frequency (MHz)</th>
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<tbody>
<tr>
<td>GPS L1/QZSS</td>
<td>1575.42 ± 1 MHz</td>
</tr>
<tr>
<td>GPS L1C, Galileo E1, Compass B1-BOC</td>
<td>1575.42 ± 2 MHz</td>
</tr>
<tr>
<td>GPS L1 wide</td>
<td>1575.42 ± 10 MHz</td>
</tr>
<tr>
<td>GLONASS R1</td>
<td>1602 ± 4 MHz</td>
</tr>
<tr>
<td>Compass B1</td>
<td>1561 ± 2 MHz</td>
</tr>
</tbody>
</table>

3.2 WGR7640 RF receiver pin assignments

GNSS RF ports are grouped together (purple squares)
- Sensitive RF signals
- RF front-end (filters, etc.) located in this direction as seen in the top view
GNSS baseband (green squares)
- Sensitive analog signals
- Opposite side away from RF pins

Figure 3-1 WGR RF receivers
- APQ source located in this direction as seen in the top view

<table>
<thead>
<tr>
<th></th>
<th>1</th>
<th>2</th>
<th>3</th>
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<tbody>
<tr>
<td></td>
<td>GND</td>
<td>RF_P</td>
<td>GND</td>
</tr>
<tr>
<td>4</td>
<td>RF_M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>6</td>
<td>BB_I_M</td>
<td></td>
<td></td>
</tr>
<tr>
<td>7</td>
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<tr>
<td>8</td>
<td></td>
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<td>SSBI</td>
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<td>BB_I_P</td>
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<td>10</td>
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<td>12</td>
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<tr>
<td>13</td>
<td>VDD_RF_1P3</td>
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<td>14</td>
<td>BB_Q_P</td>
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<td>15</td>
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<td>16</td>
<td>VDD_RF_1P3</td>
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<tr>
<td>17</td>
<td>VDD_DIG_1P8</td>
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</table>

Figure 3-2 WGR7640 RF receiver pin assignments
4 WGR IC Details – Baseband Interfaces

4.1 WGR Rx baseband interfaces with Application Processor Qualcomm (APQ) IC

The baseband interface has two differential pairs: in-phase (I) and quadrature (Q):

- The I and Q baseband outputs are sensitive analog signals.
- Route the I and Q signals as phase-critical differential pairs.
- The resistance and capacitance on each pair should be equal.
- Avoid crossing these traces; if necessary, cross them only near the APQ end points.
  - Isolate the device from digital logic and clock traces with ground all around; treat similarly to controlled-impedance traces.
  - The length of the I/Q traces between the APQ and WGR should be equal and should not exceed 8 inches.

4.2 WGR RF GNSS input ports – schematic

Optional:

- An external LNA (not required)
- Space and pads for an external LNA preceded by a second bandpass filter (to allow addition of these components if necessary)
4.3 WGR RF GNSS input ports – layout guidelines

- Traces from the filters (pink arrows) must use controlled-impedance techniques – microstrip or stripline – designed to provide 100 Ω differential (nominal). Stripline provides higher isolation since it is surrounded by ground planes.
- The components are close to the WGR pins; routing is short and direct.
- If needed, the areas directly below all component pads and signal traces are cleared of metal on layer 2 to minimize parasitic capacitance (not shown).
- Inductors should be placed in ways that limit mutual coupling.
- The complementary paths within each differential pair should be as symmetrical as possible to preserve their phase balance and maintain common-mode rejection.
- Where possible, isolate matching components and traces from all other circuits and traces using coplanar ground fill (not shown).
- Trace capacitances between WGR input pins and matching components should be kept very low.
- Some extra components are included in initial layouts to increase matching flexibility but might prove unnecessary after careful testing and evaluation.
- Specific RF grounding guidelines should be followed:
  - The ground side of the RF components must connect as directly as possible to the nearest ground reference and should connect to multiple ground fills on multiple layers to provide the best grounding.
  - Do not allow long, thin traces to connect RF components to ground – the added trace inductance could disrupt circuit performance.
  - Microvias from the ground pads directly to the PCB ground plane are recommended.
  - A total ground inductance of less than 100 pH is desired.
4.4 GNSS receiver matching procedure

- Measure the differential 100 Ω input return loss (Sdd11) looking into the WGR device’s matching network.

- Iteratively adjust the matching network with minor component changes to achieve the desired performance, making trade-offs between the following objectives as needed:
  - Center the passband and provide sufficient bandwidth.
  - Minimize the nominal noise figure using sensitivity measurements.
  - Standard values of inductors and capacitors can be selected.
  - The type and size of inductors can affect noise figure.

![Diagram of GNSS receiver matching](image)

Figure 4-4 GNSS receiver matching
5 WGR IC Details – Support Circuits

5.1 WGR support circuits high-level comments

- WGR pins and circuits that provide secondary support functions to the RF transceiver include:
  - GNSS LO synthesizer and related
  - 19.2 MHz XO input
  - Digital status and control signals
  - Single-wire serial bus interface (SSBI)

- Grounds
  - Pins 1 and 3 – grounded via a 0 Ω resistor

![WGR7640 Support Circuits Diagram]

Figure 5-1 WGR support circuits

5.2 GNSS LO synthesizer

- The integrated local oscillator (LO) generation and distribution circuits are driven by internal VCOs to support various modes to yield highly flexible quadrature LO outputs to the GNSS down converter.

- The WGR7640 IC has a dedicated synthesizer used for GNSS operation. This synthesizer provides the LO for the GNSS receiver.
- For the WGR7640 IC, an external 19.2 MHz input signal obtained from the PMIC device is required to provide the synthesizer frequency reference to which the PLL is phase- and frequency-locked.

- The WGR7640 IC integrates all of the PLL loop filter components on-chip. With the integrated PLL synthesizers, the WGR7640 IC has the advantage of more flexible loop bandwidth control, fast lock time, and low integrated phase error.

![Diagram of WGR7640 IC GNSS LO synthesizer](image)

**Figure 5-2 GNSS LO synthesizer**

### 5.3 WGR digital status and control

- **Power (VDD_DIG_1P3)** – Use the same supply that is used for APQ digital I/Os to ensure logic compatibility and prevent latchups.

- **SSBI** allows efficient initialization, GNSS mode and parameter controls, and programming verification:
  - The APQ device’s SSBI controller is the master while the WGR circuit is the slave.
  - SSBI is clocked at 19.2 MHz (reference clock frequency), so good layout techniques are extremely important.

- The SSBI signal is decoded and used to set on-chip control signals to the GNSS functional blocks. GNSS status is also reported to the APQ device through these circuits and SSBI.
Primary IC operating modes, such as sleep, warmup, air interface technology, etc.

Circuit parameters such as gain, bias conditions, on/off, clock rates, LO frequencies, etc.

RF transceiver status & control

Supports GNSS functions

Other I/Os

Primary status & control signaling

Figure 5-3 WGR digital status and control
6 Top-level Design Topics

6.1 Top-level parts placement WGR

1. Place the WGR section as close as possible to the GNSS antenna.
2. Digital devices and traces must not be placed near the top edge because they generate noise that could couple onto antennas, degrading performance (self-jamming/spurs).
3. Isolate the power management circuitry – especially SMPS circuits – from the WGR circuits.
4. The 19.2 MHz clock trace between the WGR7640 and PM8921 should be well isolated.
5. Allow space for shields. Specific shielding guidelines are given next.

Figure 6-1 Top-level parts placement WGR
6.2 Shielding recommendations

- Shield the WGR7460 IC, its matching components, RF front end components, digital (including the APQ device), and PMIC circuits.
- Metal cans are better than metallized plastic.
- Recommended shield partitioning:
  - Preserve Tx-to-Rx isolation
  - WGR IC and its Rx matching components in one shield and RF front end components in another shield
  - Do not locate WGR matching inductors too close to shield walls (this might cause EM coupling and inductor de-Q)

6.3 WGR DC power topology

- The number of bypass capacitors required in a final design depends upon the PCB layout:
  - Initial designs should begin with “extra” series components (such as resistors, inductors, or beads) and bypass capacitors.
  - After extensive test and evaluation, their numbers might be reduced prior to production.
  - Ground bypass capacitors with vias that are connected directly to the internal PCB RF ground plane.
  - Avoid thin, high-inductance traces.

Figure 6-2 WGR DC power topology
6.4 WGR IC DC routing and bypassing – general

- WGR IC and bypass capacitor on the same side
  - Star configuration with dedicated traces from capacitor to each WGR IC pin
  - Daisy-chain configuration with shared traces from capacitor to multiple WGR IC pins

- WGR IC and bypass capacitor on opposite sides
  - Opposite side bypassing is better due to lower loop inductance

6.5 WGR ground connections

Proper grounding is crucial:
- Dedicate at least one layer for ground – layer 5 is shown for example
- Ground plane – common point referenced by all handset circuits
- Fill unused space on all layers to provide robust layer-to-layer ground
- Connect bypass caps directly to surface ground fill, with multiple vias to layer 5 ground

Keep WGR ground pins separate from all other circuit grounds until they converge on layer 5:
- Via each set as directly as possible to the layer 5 ground plane.
- Include as much ground fill as possible to each layer between 1 and 5 below the WGR device, connecting each stack of vias to the WGR ground fill areas.
- Use a large copper mass to provide the best possible electrical ground and thermal conductivity – both needed for WGR performance.
Below the WGR device – isolate WGR grounds from all others on all layers except the PCB ground plane layer. The two grounds are tied together ONLY on the PCB ground layer.

Figure 6-3 WGR ground connections
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