WCN3620 Layout Guidelines

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<tr>
<th>Revision</th>
<th>Date</th>
<th>Description</th>
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<tr>
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<td>September 2016</td>
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<td>Initial release</td>
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1 Introduction

This document’s layout examples are based on a design example schematic (LM80-P0436-27). These guidelines are required to ensure WCN performance.

1.1 Purpose

This document provides guidelines for PCB designers when creating a board containing the WCN3620 IC. It is recommended that board designers should start with the reference layout and make as few changes as possible when using WCN3620 IC.

1.2 Acronyms, abbreviations, and terms

Table 1-1 provides definitions for the acronyms, abbreviations, and terms used in this document.

<table>
<thead>
<tr>
<th>Term</th>
<th>Definition</th>
</tr>
</thead>
<tbody>
<tr>
<td>BPF</td>
<td>Bandpass Filter</td>
</tr>
<tr>
<td>BT</td>
<td>Bluetooth</td>
</tr>
<tr>
<td>CLK</td>
<td>Clock</td>
</tr>
<tr>
<td>EVM</td>
<td>Error Vector Magnitude</td>
</tr>
<tr>
<td>FEM</td>
<td>Front-End Module</td>
</tr>
<tr>
<td>FM</td>
<td>Frequency Modulation</td>
</tr>
<tr>
<td>GND</td>
<td>Ground</td>
</tr>
<tr>
<td>I/O</td>
<td>Input/Output</td>
</tr>
<tr>
<td>MTP</td>
<td>Modem Test Platform</td>
</tr>
<tr>
<td>PA</td>
<td>Power Amplifier</td>
</tr>
<tr>
<td>PCB</td>
<td>Printed Circuit Board</td>
</tr>
<tr>
<td>PLL</td>
<td>Phase-Locked Loop</td>
</tr>
<tr>
<td>PMIC</td>
<td>Power Management Integrated Circuit</td>
</tr>
<tr>
<td>RF</td>
<td>Radio Frequency</td>
</tr>
<tr>
<td>RFIO</td>
<td>Radio Frequency Input and Output</td>
</tr>
<tr>
<td>Rx</td>
<td>Receive</td>
</tr>
<tr>
<td>Tx</td>
<td>Transmit</td>
</tr>
<tr>
<td>VCO</td>
<td>Voltage Controlled Oscillator</td>
</tr>
<tr>
<td>VDD</td>
<td>system supply voltage</td>
</tr>
<tr>
<td>Term</td>
<td>Definition</td>
</tr>
<tr>
<td>------</td>
<td>----------------------------</td>
</tr>
<tr>
<td>WCN</td>
<td>Wireless Computer Network</td>
</tr>
<tr>
<td>WLAN</td>
<td>Wireless Local Area Network</td>
</tr>
<tr>
<td>XO</td>
<td>Crystal Oscillator</td>
</tr>
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## 2 Pin Assignment

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<th>Description</th>
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<tr>
<td>2</td>
<td>GND</td>
</tr>
<tr>
<td>3</td>
<td>VDD_BT_RF_1P3</td>
</tr>
<tr>
<td>4</td>
<td>VDD_BT_DA_3P3</td>
</tr>
<tr>
<td>5</td>
<td>WL_BT_RFIO</td>
</tr>
<tr>
<td>6</td>
<td>WL_CMD_SET</td>
</tr>
<tr>
<td>7</td>
<td>VDD_BT_VCO_1P3</td>
</tr>
<tr>
<td>8</td>
<td>GND</td>
</tr>
<tr>
<td>9</td>
<td>VDD_WL_2GLNA_1P3</td>
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<tr>
<td>10</td>
<td>GND</td>
</tr>
<tr>
<td>11</td>
<td>VDD_WL_2GPA_3P3</td>
</tr>
<tr>
<td>12</td>
<td>GND</td>
</tr>
<tr>
<td>13</td>
<td>VDD_BT_BB_1P3</td>
</tr>
<tr>
<td>14</td>
<td>GND</td>
</tr>
<tr>
<td>15</td>
<td>NC</td>
</tr>
<tr>
<td>16</td>
<td>VDD_BT_PLL_1P3</td>
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<tr>
<td>17</td>
<td>GND</td>
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<tr>
<td>18</td>
<td>BT_CTL</td>
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<td>GND</td>
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<td>22</td>
<td>VDD_IO_1P8</td>
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<td>23</td>
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<td>24</td>
<td>VDD_XO_1P8</td>
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<tr>
<td>25</td>
<td>GND</td>
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<td>VDD_XO_PLL_1P3</td>
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<td>27</td>
<td>GND</td>
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<tr>
<td>28</td>
<td>BT_DATA</td>
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<td>29</td>
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<tr>
<td>30</td>
<td>XO_IN</td>
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<tr>
<td>31</td>
<td>NC</td>
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<tr>
<td>32</td>
<td>GND</td>
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<tr>
<td>33</td>
<td>BT_SSBI</td>
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<tr>
<td>34</td>
<td>GND</td>
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<tr>
<td>35</td>
<td>GND</td>
</tr>
<tr>
<td>36</td>
<td>VDD_WL_LO_1P3</td>
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<tr>
<td>37</td>
<td>VDD_WL_2GPA_3P3</td>
</tr>
<tr>
<td>38</td>
<td>NC</td>
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<tr>
<td>39</td>
<td>GND</td>
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<tr>
<td>40</td>
<td>NC</td>
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<td>41</td>
<td>FM_SSBI</td>
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<tr>
<td>42</td>
<td>GND</td>
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<td>43</td>
<td>VDD_WL_UPC_1P3</td>
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<td>45</td>
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<td>46</td>
<td>FM_DATA</td>
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<td>47</td>
<td>WL_BB_QN</td>
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<td>WL_CMD_DATA0</td>
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<td>49</td>
<td>WL_PDET_IN</td>
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<td>50</td>
<td>FM_HS_RX</td>
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<td>WL_BB_IP</td>
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<td>55</td>
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<td>56</td>
<td>VDD_FM_RXFE_1P3</td>
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<td>57</td>
<td>VDD_FM_RXBB_1P3</td>
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<tr>
<td>58</td>
<td>VDD_WL_PLL_1P3</td>
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<td>59</td>
<td>WL_BB_IN</td>
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<tr>
<td>60</td>
<td>VDD_WL_BB_1P3</td>
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<tr>
<td>61</td>
<td>WL_CMD_CLK</td>
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**Figure 2-1** WCN3620 pin assignments – top view
3 Board Information (2:n:2)

3.1 Stack up (2:n:2)

Figure 3-1 Example 2:n:2 PCB Layer Stackup

- Layer 1 – Parts placement
  - Components, RF microstrip, traces to pins on the outer rows
- Layer 2 – WCN RF ground
  - WCN ground pins and bypass capacitor grounds
- Layer 3 – WCN signals
  - Digital I/Os, analog baseband, power buses, XO, bypass caps to WCN pins on inner rows
- Layer 4 – Main PCB ground plane
4 Layout Checklist

4.1 Layout checklist

1. Component placement
2. Keep-out areas
3. VIAs
4. Analog ground
5. Analog baseband IQ signals
6. WLAN/BT RF trace
7. 3.3 V power supply
8. 1.3 V power supply
9. 1.2 V/1.8 V power supply
10. 19.2 MHz clock signal
11. High-speed digital signals
12. BPF Layer 2 GND cutout
13. Antenna routing area
14. FM RF trace
4.2 Board-level layout guidelines

One-sided board example

For a two-sided board, guidelines for trace routing under and around WCN are still valid.

WLAN IQ lines should be less than 10 cm long – they are susceptible to aggressor digital signals so keep them well isolated. Place ground via every 75 mil along with IQ lines.

Mandatory – route IQ as stripline.

Reserve area between PMIC and WCN for clean routing.
- Shared 1.3 V analog supply
  - Star route at PMIC to reduce noise leakage between ICs
- 3.3 V for WCN power amplifiers
- 1.8 V for digital I/Os
- 1.8 V for XO circuits
- Place ground via every 75 mil along with 19.2 MHz CLK trace

**Figure 4-1 APQ8016E chipset example**

4.2.1 Component placement

- Parts placement
  - RF matching components close to WCN pins
  - Filter matching components near the filter (critical)
  - Low-value VDD bypass capacitors close to their WCN pins (though RF matching components have higher priority)
  - WCN and its discrete components in a dedicated shield area
  - External coupler output (if used) must be isolated from the 2.4 GHz trace

Dedicated shield area for WCN and its discretes.

Short, direct RF routing; avoid or minimize layer transitions using vias.

Locate noisy board connectors away from the antennas.
Figure 4-2 Component placement

- WLAN, Bluetooth, and FM RF routing
  - RF microstrip or stripline must be used
  - RF matching becomes difficult if stripline is used between WCN and discrete components
  - Avoid frequent transitions between the layers
4.2.2 Keep-out areas

- On Layer 1, these keep-out areas cannot be routed by any signals.

Figure 4-3 Keep-out areas
In addition to these mandatory keep-out areas, layer 1 below the IC should be as clear as possible, using microvias and lower layers for routing.

**Figure 4-4  WCN3620 outer layer keep-out areas**

### 4.2.3 Vias on WCN3620

**Layer 1/2:**
- VIA 1-2

**Layer 2/3:**
- VIA 2-3

**Layer 3:**
- VIA3-6

**Figure 4-5 Vias on WCN3620**
4.2.4 Analog ground

Pin 25 and pin 35 are the analog ground pins and they need to be isolated from the other digital ground pins.

Figure 4-6 Analog ground

4.2.4.1 Ground connections

Ground connections checklist:

- Follow the mandatory keep-out areas on Layer 1 under the IC.
- There should be no Layer 1 ground pour below the IC.
- Provide a solid, continuous ground flood (WCN RF ground) on Layer 2 below the IC.
- Connect the IC ground pins and bypass capacitors’ ground pads directly to the WCN RF ground on Layer 2 using micro-vias at each pin or pad (critical).
- Using the lower layer (main PCB ground plane) for ground return increases the loop inductance and might make bypassing less effective.
4.2.5 Analog baseband I/Q signals

**Critical:** Baseband I/Q

- Keep the I/Q trace pairs equal length, symmetric, and well isolated. Maintain equal lengths for all signals within 40 mil.
- The resistance and capacitance on each pair should be equal; the total capacitance should be less than 10 pF.
- Crosstalk should be less than 60 dB at 50 MHz.
- Add GND with GND vias between two signal pairs every 75 mil from the WCN to the APQ chipset.
- Keep the I/Q signals away from the RF routing area, high-speed digital and clock signals.
- Use the same number of vias for each differential.

**Figure 4-7 Layer 3 baseband IQ Signals**
4.2.6 WLAN/BT RF trace

- Keep the RF trace at 50 Ω (critical).
- Use Layer 2 as the reference ground from the WCN to the RF connector.
- Use Layer 3 as the reference ground from the RF connector to the antenna.

Figure 4-8 WLAN/BT RF trace
4.2.7 3.3 V power supply

- The total resistance between PMIC and the WCN pins must be less than 100 mΩ (critical).
- Place C1 away from pin 5 (WL_BT_RFIO), preferably close to the C4 (critical).
- Star route 3.3 V VDD traces from the shared capacitor to pin 4 (VDD_BT_DA_3P3) and pin11 (VDD_WL_2GPA_3P3) with a minimum routing distance between pins of > 5 mm (critical).
- Instability in the 2.4 GHz Tx output may occur without this recommended star routing.

Figure 4-9 3.3 V power supply
4.2.7.1 Additional 3.3 V/1.3 V power supply layout checklist

Power distribution routing:

- 3.3 V and 1.3 V high current traces should maintain a length-to-width ratio of less than 10 to maintain a maximum 0.1 Ω IR drop from the PMIC to the WCN pins (extremely critical).
  - Failure to maintain this ratio can cause Tx EVM degradation.
- Route supply voltage rails from the PMIC to the inner layers.
- Keep all supply traces away from the RF pin 5 (WL_BT_RFIO) and RF traces.
- Isolate the 1.3 V and 3.3 V traces from each other; do not route in parallel.
- Do not run supply traces from one side of the WCN3620 through the WCN3620 to the other side; it is recommended to run the supply trace around the WCN3620 and then have a short trace from the outside directly to the WCN3620 supply pins.
- Route to bypass capacitors first and then continue route to the WCN pin.

4.2.7.2 Recommended RF trace routing and 3.3 V bypass cap placement

![Good isolation between RFIO and 3.3 V WLAN PA supply](image)

**Figure 4-10 RF Trace Routing**

- It is highly recommended to have good isolation between the RFIO and 3.3 V WLAN PA supply (extremely critical).
- For 2G RF trace, it is recommended to route it to the west directly and connect to the RF connector.
4.2.7.3 Examples of Incorrect Layout

Figure 4-11 shows two examples of poor isolation between RFIO and the 3.3 V WLAN PA supply.

No isolation between RFIO and 3.3 V supply! No isolation between RFIO and 3.3 V supply!

Bad example 1
Bad example 2

Figure 4-11 Examples of Incorrect Layout
4.2.8 1.3 V power supply

- The total resistance from PMIC to the WCN pins must be less than 100 mΩ (critical).
- It is recommended to have minimum 20 mil trace width with shortest length between PMIC to WCN.
- Figure 4-12 shows the overall 1.3 V routing.
4.2.9 1.2 V/1.8 V power supply

Figure 4-13 1.8V Supply Routing
4.2.10 19.2 MHz clock signal

Clock trace routing:

- Route the 19.2 MHz system clock with isolated inner-layer traces all the way from the PMIC to the WCN pin (critical).

**NOTE:** The PMIC 19.2 MHz clock is the only clock source for WCN3620. This signal needs to be well isolated/protected.

- Keep clock traces away from any supply, I/Q, and RF traces.
- Keep 10 mil keep-out from GND copper pour.
- 19.2 MHz clock trace should be routed away from FM RF trace to avoid FM desense at 96 MHz.
4.2.11 High-Speed digital signals

<table>
<thead>
<tr>
<th>Pad</th>
<th>Signals</th>
<th>Routing guide</th>
</tr>
</thead>
<tbody>
<tr>
<td>61</td>
<td>WL_CMD_CLK</td>
<td>▪ WLAN 5-wire control bus</td>
</tr>
<tr>
<td>6</td>
<td>WL_CMD_SET</td>
<td>▪ Route signals in inner layers and away from RF signals, I/Q analog signals,</td>
</tr>
<tr>
<td>48</td>
<td>WL_CMD_DATA0</td>
<td>and XO signal</td>
</tr>
<tr>
<td>26</td>
<td>WL_CMD_DATA1</td>
<td></td>
</tr>
<tr>
<td>55</td>
<td>WL_CMD_DATA2</td>
<td></td>
</tr>
<tr>
<td>30</td>
<td>19.2 MHz clock signal (XO)</td>
<td>▪ Route in the inner layer</td>
</tr>
<tr>
<td></td>
<td></td>
<td>▪ Keep 10 mil keep-out from GND copper pour</td>
</tr>
<tr>
<td>18</td>
<td>BT_CTL</td>
<td>▪ BT 3-wire control/data bus</td>
</tr>
<tr>
<td>33</td>
<td>BT_SSBI</td>
<td>(9.6 MHz)</td>
</tr>
<tr>
<td>28</td>
<td>BT_DATA</td>
<td></td>
</tr>
<tr>
<td>41</td>
<td>FM_SSBI</td>
<td>▪ FM 2-wire control/data bus</td>
</tr>
<tr>
<td>46</td>
<td>FM_DATA</td>
<td>(9.6 MHz)</td>
</tr>
</tbody>
</table>

Figure 4-15 WLAN 5 wire bus on Layer 3

High-speed digital signal routing:

- Keep the high-speed digital signals of equal length or within 100 mil.
- Keep the high-speed digital signals away from any supply, I/Q, and RF traces.
- Keep 10 mil keep out from the GND copper pour.

4.2.11.1 BT digital signals

Figure 4-16 BT Data Signal Routing
4.2.11.2 FM digital signals

![Layer 2 (FM_SSBI & FM_DATA)](image1) ![Layer 3 (FM_SSBI & FM_DATA)](image2) ![Layer 2 & 3](image3)

Figure 4-17 FM Digital Signal Routing

4.2.12 BPF Layer 2 GND cutout

![Layer 1](image4) ![Layer 2](image5) ![Layer 3](image6)

Figure 4-18 Bandpass Filter
4.2.13 Antenna routing area

The antenna routing area must be as similar as possible to the one shown in Figure 4-19.

Figure 4-19 Antenna Routing Area
4.2.14 FM RF trace

- The FM matching/WAN filtering components should be placed close to the chip.
- For a Murata connector, there should be no ground copper pour on layers 1, 2, and 3.
4.3 Summary (Layer 1)

Layer 1 note:
- No ground pour below WCN3620
- BT/WL RF trace
- FM RF trace
- 1.3 V power supply trace
- 3.3 V power supply trace
- 1.8 V IO trace
- BT digital signals (BT data/BT SSBI)

Separate the ground pads of C4 and C7 and use a dedicated...
4.4 Summary (Layer 2)

Layer 2 note:
- Needs a solid/continuous ground underneath WCN3620
- Analog ground island
- 1.3 V power supply trace
- FM digital signals
- BPF ground cutout area (follow vendor’s recommendation)
4.5 Summary (Layer 3)

Layer 3 note:
- Analog ground island
- Analog IQ signals
- 1.3 V power supply trace
- 3.3 V power supply trace
- 1.2 V/1.8 V power supply trace
- XO
- WLAN 5 wire bus
- BT digital signal
- FM digital signals
5 Layout Guidelines for 1:n:1 Stack Up

5.1 Layer usage

- This guideline is created for 1-4-1 or 1-6-1 stack up.
- Use four layers designated to WCN.
- The instance name is based on the reference schematic.
  - L1 (Top): RF trace and supply
  - L2: RF ground, supply and WCN signals
  - L3: System ground
  - L4: For cleaner routing, L4 can be used for digital signals and 3.3 V/1.3 V supply if L4 is available

![Layer Diagram](image)

**Figure 5-1 Stackup for 1:N:1**

**NOTE:** Clear up all four layers around the chip before starting the work!
1. Place and route RF components and WLAN PA bypass caps.

   - Good isolation between RFIO and 3.3 V PA supply
     - **PUT GND POUR!!**
     - L1
     - L2
     - L3
     - L4
     - L2 C64
     - Place FM matching close to the chip
     - Connect shunt cap GND to inner layer and clean GND

2. Route BT 3.3 V.

   - Star route 3.3 V VDD traces from the shared capacitor to pin 4 (VDD_BT_DA_3P3) and pin 11 (VDD_WL_2GPA_3P3) with a minimum routing distance between pins of > 5 mm. Otherwise, Tx spur issue shows up
     - **NEVER DO THIS!**
3. Route 1.3 V VDDs.

4. Route 1.8 V and 1.2 V VDDs.
5. Connect PA/LNA GNDs.

**Note:** VIA12 to L2 for pins 1/2/8/12/17/39/44/45/10/19/20/21/42 are not shown in this drawing.

Do not connect three GNDs on top layer, if possible.

Add as many GND vias as possible.

6. Connect WL PLL/VCO GNDs.
7. Connect FM GNDs.

* Connect pin 34 with pin 39 using top layer to make room for CLK.
8. Connect BT GNDs.

a. Check point: VDD-GNDs are all connected.
9. Connect analog IQ and XO.

10. Connect CLK.
11. Connect digital signals on.

12. Connect main 1.3 V and 3.3 V line.
EXHIBIT 1

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