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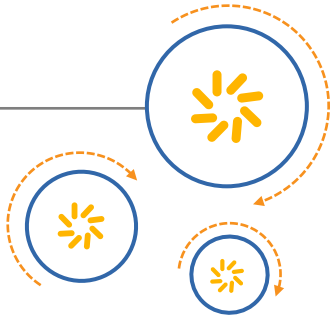

Qualcomm® Snapdragon™ 600E Processor APQ8064E
Recommended Memory Controller and Device Settings

Application Note

September 2016

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LM80-P0598-6 Rev.B

Revision history

Revision	Date	Description
B	September 2016	Update for ‘E’ part
A	May 5, 2015	Initial release

Contents

Tables

1 Introduction

1.1 Purpose

This document provides the recommended EBI0/EBI1 register settings for modules and solutions based on the Qualcomm® Snapdragon™ 600E (APQ8064E) processor. It is strongly advised to follow these settings to alleviate stability and performance concerns.

1.2 Scope

This document provides specific values that must be set for different EBI0/EBI1 registers to achieve stable performance for standard LPDDR2/PCDDR3 SDRAM on the reference platform.

NOTE: This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE: Enabling some features may require additional licensing fees.

2 Recommended EBI0/EBI1 register settings

Specific settings must be performed to initialize the external memory on EBI0/EBI1 into a stable, usable state. These settings may be on the device itself (see Section 2.1.2), or on the APQ8064E chipset (see Section 2.1.3). This chapter provides the recommended EBI0/EBI1 register settings based on the device characteristics of the external memory device, as well as the APQ8064E settings provided in Section 2.1.1. The settings must be adjusted accordingly when device characteristics differ from the values listed in Section 2.1.1.

Only the recommended settings are provided in this chapter. Users should refer to the memory device manufacturer's datasheet.

This document applies to APQ8064E based devices when used with a dual-channel 2-die LPDDR2 (2 x 512 MB) and dual channel 4-die PCDDR3 (4 x 256 MB) configuration.

2.1 APQ8064E EBI0/EBI1 register settings for LPDDR2 devices

The recommended settings in this document are intended to support the Snapdragon 600E (APQ8064E) processor with the 533 MHz LPDDR2 SDRAM clock frequency.

2.1.1 Device characteristics

Table 2-1 lists the key device characteristics required to set up the EBI registers. The values supply information (for example, clock speed), temperature parameters, and organization parameters. Refer to the device's datasheet for more details on how to adjust the device settings based on the characteristics.

Table 2-1 EBI LPDDR2 SDRAM interface information

Parameter	Value	Unit
DDR_CLK_Freq	533	MHz
XO_Freq	27	MHz
LPDDR2 SDRAM device parameters		
tRPpB	18	ns
tRPaB	21	ns

Parameter	Value	Unit
tWR	15	ns
tRRD	10	ns
tWTR	7.5	ns
tXP	7.5	ns
tCKE	3	tCK
tRFC	130	ns
tRCD	18	ns
tRAS	42 (min)	ns
	70,000 (max)	
tRC	63	ns
tXSR	140	ns
tFAW	50	ns
tRTP	7.5	ns
RL	8	tCK
WL	4	tCK
tDQSCK	2.5 (min)	ns
	5.5 (max)	
tREFIab	3.9	µs
tREFIpb	0.4875	µs
tREFW	32	ms
tINIT2	5	tCK
tINIT3	200	µs
tINIT4	1	µs
tMRR	2	tCK
tZQCL	360	ns
tZQCS	90	ns
tZQINIT	1	µs

Parameter	Value	Unit
tMRW	5	tCK
tCKESR	15	ns
tZQRESET	50	ns
tREFBW	4.16	µs
tDQSQ	0.20	ns
tQHS	0.23	ns
Number of rows (CS0)	16384	
Number of columns (CS0)	1024	
Number of banks (CS0)	8	
Number of rows (CS1)	16384	
Number of columns (CS1)	1024	
Number of banks (CS1)	8	
Number of required refreshes R	8192	
Burst length	4	
Device density (CS0)	512	MB
Device density (CS1)	512	MB

NOTE: All the specifications listed in Table 2-1 are based on the Samsung K3PE0E000A-XGC2 LPDDR2 device. Embedded designers are responsible for using appropriate specification values corresponding to the LPDDR2 devices of interest.

2.1.2 Recommended settings for EBI0/EBI1 mode configuration

DDR_MR_CNTL_WDATA sets the SDRAM device into a specific mode. They also define device operation behaviors, e.g., burst length, drive strength, or partial refresh settings. Refer to the memory device manufacturer's data sheet for details about mode registers.

2.1.3 Recommended settings for APQ8064E registers

Table 2-2 provides recommended settings for clock frequency-independent registers.

Table 2-2 Clock frequency-independent registers

Offset	Register name	Bits	Field name	Value
0x00004	TOP_MISC_CNTL	31:0	–	0x0004F0EC
		31:21	Reserved	0
		20	IOCAL_UPDATE_METHOD	0
		19:16	IOCAL_UPDATE_PULSE_WIDTH	4
		15	CLKON_DDR_PIPE_MANUAL	1
		14	MODE_CLKON_DDR_PIPE	1
		13	CLKON_DDR_2X_MANUAL	1
		12	MODE_CLKON_DDR_2X	1
		11	MODE_MEM_HALT	1
		10:8	Reserved	0
		7	CLKON_AHB_MANUAL	1
		6	MODE_CLKON_AHB	1
		5	CLKON_DDR_1x_MANUAL	1
		4	MODE_CLKON_DDR_1x	0
		3	CLKON_AXI_MANUAL	1
		2	MODE_CLKON_AXI	1
		1:0	Reserved	0
0x40000	SLV_CONFIG	31:0	–	0x01001007
		31	CLKON_DISABLE	0
		30:26	Reserved	0
		25:16	CLKON_IDLE_TIMER	256
		15:14	Reserved	0
		13:12	INTERLEAVE	1
		11:10	Reserved	0

Offset	Register name	Bits	Field name	Value
		9:8	CMD_ORDERING	0
		7:3	Reserved	0
		2:0	CMD_Q_DEPTH	7
0x40004	SLV_RD_CONFIG	31:0	–	0x000B003F
		31:22	Reserved	0
		21:16	RD_CMD_FIFO_DEPTH	11
		15:6	Reserved	0
		5:0	RD_DATA_FIFO_DEPTH	63
0x40008	SLV_RD_STATUS (RD)	31:0	–	0x00000000
		31:28	Reserved	0
		27:24	RDQUAL_FIFO_ENTRIES_IN_USE	0
		23:16	RDDATA_FIFO_ENTRIES_IN_USE	0
		15:8	RDDATA_FIFO_EMPTY	0
		7:1	Reserved	0
		0	DQS_ERROR	0
0x4000C	SLV_WR_CONFIG	31:0	–	0xC708040F
		31	COALESCE_EN	1
		30	READ_MERGE_EN	1
		29	FLUSH	0
		28	EMPTY	0
		27	WRITE_BLOCK_READ	0
		26:24	CMD_BUF_DEPTH	7
		23:21	Reserved	0
		20:16	FLUSH_UPPER_LIMIT	8
		15:13	Reserved	0
		12:8	FLUSH_LOWER_LIMIT	4
		7:5	Reserved	0

Offset	Register name	Bits	Field name	Value
		4:0	WR_BUFFER_DEPTH	15
0x40010	SLV_FLUSH_CONFIG	31:0	–	0x00008010
		31:30	FLUSH_PRIORITY	0
		29	Reserved	0
		28	FLUSH_IN_ORDER	0
		27:18	Reserved	0
		17:8	FLUSH_IDLE_DELAY	128
		7:0	PAGE_HIT_WINDOW	16
0x40014	SLV_ID_REVISION (RD)	31:0	–	0x00005310
		31:16	Reserved	0
		15:12	REV_MAJOR	5
		11:08	REV_MINOR	3
		7:4	SITE_ID	1
		3:0	Reserved	0
0x40020	SLV_ADDR_BASE_CS0	31:0	–	0x00008000
		31:16	Reserved	–
		15:8	BASE_ADDR	128
		7:0	Reserved	0
0x40024	SLV_ADDR_BASE_CS1	31:0	–	0x0000C000
		31:16	Reserved	–
		15:8	BASE_ADDR	192
		7:0	Reserved	–
0x40030	SLV_ADDR_MAP_CS0	31:0	–	0x00008122
		31:16	Reserved	0
		15	RANK_EN	1
		14	Reserved	0
		13:12	ADDR_MAP_MODE	0

Offset	Register name	Bits	Field name	Value
		11:9	Reserved	0
		8	NUM_BANK	1
		7:6	Reserved	0
		5:4	WIDTH_ROW	2
		3:2	Reserved	0
		1:0	WIDTH_COL	2
0x40034	SLV_ADDR_MAP_CS1	31:0	–	0x00008122
		31:16	Reserved	0
		15	RANK_EN	1
		14	Reserved	0
		13:12	ADDR_MAP_MODE	0
		11:9	Reserved	0
		8	NUM_BANK	1
		7:6	Reserved	0
		5:4	WIDTH_ROW	2
		3:2	Reserved	0
		1:0	WIDTH_COL	2
0x40040	SLV_ADDR_SIZE_MASK_CS0	31:0	–	0x0000E000
		31:16	Reserved	0
		15:8	ADDR_MASK	224
		7:0	Reserved	0
0x40044	SLV_ADDR_SIZE_MASK_CS1	31:0	–	0x0000E000
		31:16	Reserved	0
		15:8	ADDR_MASK	224
		7:0	Reserved	0

Offset	Register name	Bits	Field name	Value
0x40050	SLV_STALL	31:0	–	0x00000004
		31:3	Reserved	0
		2	AXI_IDLE	1
		1	STALL_ACK	0
		0	STALL_REQ	0
0x40100	SLV_ERR_ADDR (RD)	31:0	–	0x00000000
		31:0	ERR_ADDR	0
0x40108	SLV_ERR_APACKET_0 (RD)	31:0	–	0x00000000
		31:16	Reserved	0
		15:0	ERR_AMID	0
0x4010C	SLV_ERR_APACKET_1 (RD)	31:0	–	0x00000000
		31:28	Reserved	0
		27:24	ERR_ALEN	0
		23:16	ERR_ATID	0
		15:13	ERR_ASIZE	0
		12	ERR_ABURST	0
		11:8	ERR_ATYPE	0
		7:6	ERR_ALOCK	0
		5:4	Reserved	0
		3	ERR_APROTNS	0
		2	ERR_AOOORD	0
		1	ERR_AOOOWR	0
		0	ERR_AWRITE	0
0x40114	SLV_ERR_CNTL	31:0	–	0x00001000
		31:13	Reserved	0
		12	IRQ_EN	1
		11:9	Reserved	0

Offset	Register name	Bits	Field name	Value
		8	CLEAR_ERR	0
		7:5	Reserved	0
		4	ERR_OCCURRED	0
		3:2	Reserved	0
		1:0	ERR_CODE	0
0x80000	DDR_DEVICE_CONFIG	31:0	–	0x0F004113
		31:28	Reserved	0
		27:26	DEVICE_CONFIG_RANK1	3
		25:24	DEVICE_CONFIG_RANK0	3
		23:18	Reserved	0
		17	INIT_DONE_RANK1	0
		16	INIT_DONE_RANK0	0
		15:14	NUM_BANKS	1
		13:12	Reserved	0
		11:10	CLK_SYNC_MODE	0
		9:7	DEVICE_TYPE	2
		6	Reserved	0
		5	MEM_CLK_CONFIG	0
		4	DDR_COMMAND_BUS	1
		3:2	Reserved	0
		1	RANK1_EN	1
		0	RANK0_EN	1
0x80004	DDR_DEVICE_STATUS (RD)	31:0	–	0x00000000
		31:18	Reserved	0
		17	INTERRUPT_EN	0
		16	CURR_SEL_REG_FREQ_SWITCH	0
		15:14	Reserved	0

Offset	Register name	Bits	Field name	Value
		13	IN_DEEP_POWER_DOWN_RANK1	0
		12	IN_DEEP_POWER_DOWN_RANK0	0
		11:10	Reserved	0
		9	IN_SELF_RFSH_RANK1	0
		8	IN_SELF_RFSH_RANK0	0
		7:6	Reserved	0
		5	RANK1_TEMP_OO_RANGE	0
		4	RANK0_TEMP_OO_RANGE	0
		3:2	Reserved	0
		1	RANK1_IDLE	0
		0	RANK0_IDLE	0
0x80010	DDR_MANUAL_CMD	31:0	–	0x00000000
		31:18	Reserved	0
		17:16	RANK_SEL	0
		15	Reserved	0
		14	CK_ON	0
		13	CKE	0
		12	RESET_N	0
		11:7	Reserved	0
		6	ENTER_DEEP_PD	0
		5	EXIT_DEEP_PD	0
		4	ZQ_CAL_SHORT	0
		3	ZQ_CAL_LONG	0
		2	AUTO_REFRESH	0
		1	PRECHARGE_ALL	0
		0	SR_READ	0

Offset	Register name	Bits	Field name	Value
0x80014	DDR_MR_CNTL_WDATA	31:0	–	0x000 00000
		31:24	MR_ADDR	0
		23:20	Reserved	0
		22	RD_DQCAL	0
		21:20	RD_DQCAL_EXP_PATTERN	0
		19:18	MR_RANK_SEL	0
		17	MRR	0
		16	MRW	0
		15:0	MR_WDATA	0
0x80020	DDR_MR_RDATA_RANK0 (RD)	31:0	–	0x00000000
		31:0	MR_RDATA	0
0x80024	DDR_MR_RDATA_RANK1 (RD)	31:0	–	0x00000000
		31:0	MR_RDATA	0
0x80028	DDR_MRR_REPEAT	31:0	–	0x0401C000
		31:24	MRR_ADDR	0
		23:19	Reserved	0
		18:16	MRR_INTERVAL	1
		15:14	MRR_RANK_SEL	3
		13:12	Reserved	0
		11:8	MRR_INTERVAL_OVERRIDE	0
		7:0	Reserved	0
0x80034	DDR_MRR_REPEAT_DATA_RANK0 (RD)	31:0	–	0x00000000
		31:0	MRR_DATA	0
0x80038	DDR_MRR_REPEAT_DATA_RANK1 (RD)	31:0	–	0x00000000
		31:0	MRR_DATA	0

Offset	Register name	Bits	Field name	Value
0x8003C	DDR_CMD_EXEC_OPT_0	31:0	–	0x00208005
		31:28	Reserved	–
		27:16	PAGE_OPEN_TIMER	32
		15	PAGE_MGMT_POLICY	1
		14:7	RDCMD_STARVATION_TIMER	0
		6	WR_RD_PREF	0
		5	DDR_CK_ALWAYS_ON_DBG_MODE	0
		4	CONCURRENT_SELF_REFRESH_EN	0
		3	SEL_REG_FREQ_SWITCH	0
		2	PWR_DOWN_EN	1
		1	CLK_STOP_EN	0
		0	CLK_STOP_DURING_PWR_DOWN_EN	1
0x80040	DDR_CMD_EXEC_OPT_1	31:0	–	0x00000339
		31:28	Reserved	0
		27	SELF_REFRESH_RANK1	0
		26	SELF_REFRESH_RANK0	0
		25:22	Reserved	0
		21:12	RANK_IDLE_TIMER	0
		11:8	RUN_ATLEAST_ONE_TRANS_RD_CONFLICT	3
		7:4	RUN_ATLEAST_ONE_TRANS_WR_CONFLICT	3
		3	ENABLE_DDR2X_CLKON_DURING_CSPD	1
		2	ENABLE_POWER_OPT_AUTO_SRR_ZQ	0
		1	ENABLE_CMD_ADDR_OE_CNTL	0
		0	LOAD_TRP_CNTL	1

Offset	Register name	Bits	Field name	Value
0x80044	DDR_CMD_EXEC_OPT_2	31:0	–	0x22040390
		31	Reserved	0
		30:28	ZQCAL_INTERVAL	2
		27:20	CLKON_IDLE_TIMER	32
		19:14	CLKON2X_ASSERT_WAIT_TIMER	16
		13:10	Reserved	0
		9:8	RDCMD_HP_REMAP_LEVEL3	3
		7:6	RDCMD_HP_REMAP_LEVEL2	2
		5:4	RDCMD_HP_REMAP_LEVEL1	1
		3:2	RDCMD_HP_REMAP_LEVEL0	0
		1:0	Reserved	0
		0	UPDATE_MEM_LATENCY_ON_FREQ_SWITCH	0
0x80048	DDR_CMD_EXEC_OPT_3	31:0	–	0x00000350
		31	CODT_ON_WR	0
		30	CODT_ON_RD	0
		29	RANK1_ODT_ON_WR_RANK1	0
		28	RANK1_ODT_ON_WR_RANK0	0
		27	RANK1_ODT_ON_RD_RANK1	0
		26	RANK1_ODT_ON_RD_RANK0	0
		25	RANK0_ODT_ON_WR_RANK1	0
		24	RANK0_ODT_ON_WR_RANK0	0
		23	RANK0_ODT_ON_RD_RANK1	0
		22	RANK0_ODT_ON_RD_RANK0	0
		21:19	ODT_START_DELAY_WR	0
		18:16	ODT_START_DELAY_RD	0
		15:13	ODT_OFF_DELAY	0

Offset	Register name	Bits	Field name	Value
		12:10	ODTH8	0
		9	EN_ODT_SWITCH_RANK_UNAVAIL	1
		8	EN_ODT_POWER_DOWN	1
		7:6	ODT_EXTEND_DELAY_WR	1
		5:4	ODT_EXTEND_DELAY_RD	1
		3:1	tANPD	0
		0	DLL_CNTL_PCHG_PD	0
0x8004C	DDR_CMD_EXEC_OPT_4	31:0	–	0x20000000
		31: 24	PWR_DOWN_IDLE_TIMER	32
		23:0	Reserved	0
0x80050	DDR_SM_TIMING_0	31:0	–	0x00002F84
		31:15	Reserved	0
		14:12	DLY_RD_DIFF_RANK	2
		11	RD_INT_BY_RD	1
		10	WR_INT_BY_WR	1
		9	RD_INT_BY_BST	1
		8	WR_INT_BY_BST	1
		7:6	WR_INT_RD_OR_PRECHG_MODE	2
		5:4	Reserved	0
		3:2	INT_BOUNDARY	1
		1:0	Reserved	0
0x80054	DDR_SM_TIMING_1	31:0	–	0x00000002
		31:24	Reserved	0
		23:20	MEM_START_BURST_RD	0
		19:16	MEM_START_BURST_WR	0
		15:14	SYS_TIMING_MODE	0
		13:8	Reserved	0

Offset	Register name	Bits	Field name	Value
		7	USE_ORIG_BL	0
		6	Reserved	0
		5	ON_THE_FLY_MODE	0
		4	DRIVE_WR_DQS_EARLY	0
		3:0	BURST_LENGTH	2
0x800A0	DDR_AUTO_RFSH_CNTL	31:0	–	0x071A1007
		31:28	Reserved	0
		27:24	COUNT_RFSH_AHEAD	7
		23	TEMP_ADJUST_RFSH	0
		22:14	TREFI	104
		13:12	MODE_AUTO_RFSH	1
		11:3	Reserved	0
		2:0	REFRESH_IDLE_ACROSS_RANKS	7
0x800A8	DDR_SELF_RFSH_CNTL	31:0	–	0x0C002000
		31:28	Reserved	0
		27	HW_SELF_RFSH_EN_RANK1	1
		26	HW_SELF_RFSH_EN_RANK0	1
		25:20	Reserved	0
		19:8	HW_SELF_RFSH_TIMER	32
		7:0	Reserved	0
0x80200	DDR_ENHPRI_EN	31:0	–	0xED900000
		31	ENHANCED_PRI_EN	1
		30	RD_PRI_AGING_EN	1
		29	WR_PRI_AGING_EN	1
		28	Reserved	0
		27	ADJ_PRI_RDBLOCKING	1
		26	ADJ_PRI_RDMERGE	1

Offset	Register name	Bits	Field name	Value
		25:24	PRI_RDBLOCKING	1
		23	ADJ_PRI_WRBLOCKING	1
		22	Reserved	0
		21:20	PRI_WRBLOCKING	1
		19:16	Reserved	0
		15:8	CONFLICT_BLOCK_HIT	0
		7	Reserved	0
0x80224	DDR_ENHPRI_RD1	31:0	–	0x00000008
		31:7	Reserved	0
		6:0	CYCLES_AXIPRI0	8
0x80228	DDR_ENHPRI_RD2	31:0	–	0x00000000
		31:7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x8022C	DDR_ENHPRI_RD3	31:0	–	0x00000800
		31:15	Reserved	0
		14:8	CYCLES_AXIPRI1	8
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80230	DDR_ENHPRI_RD4	31:0	–	0x00004040
		31:15	Reserved	0
		14:8	CYCLES_AXIPRI1	64
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	64
0x80234	DDR_ENHPRI_RD5	31:0	–	0x00000000
		31:23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	0

Offset	Register name	Bits	Field name	Value
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80238	DDR_ENHPRI_RD6	31:0	–	0x00000000
		31:23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x8023C	DDR_ENHPRI_RD7	31:0	–	0x00000000
		31	Reserved	0
		30:24	CYCLES_AXIPRI3	0
		23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80248	DDR_ENHPRI_WR2	31:0	–	0x00000000
		31:7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80250	DDR_ENHPRI_WR4	31:0	–	0x00000040
		31:15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	64

Offset	Register name	Bits	Field name	Value
0x80258	DDR_ENHPRI_WR6	31:0	–	0x00000000
		31:23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	–
		14:8	CYCLES_AXIPRI1	–
		7	Reserved	–
		6:0	CYCLES_AXIPRI0	0
0x0E0	DIM_CA_IOC_CTLR_CFG	31:0	–	0x4101071F
		31	CAL_NOW	0
		30	IO_CAL_AUTO	1
		29	IO_CAL_FF_TIMER_EN	0
		28	IO_CAL_BANDGAP_DYN_CTRL	0
		27:26	Reserved	0
		25	SW_FFCLK_ON	0
		24	LV_MODE	1
		23:21	Reserved	0
		20:16	MARGIN_LOAD	1
		15:14	Reserved	0
		13:12	IMP_SEL	0
		11	Reserved	0
		10	PN_SEL_CA	1
		9	PN_SEL_DATA	1
		8	CAL_USE_LAST	1
		7	Reserved	0
		6:4	SAMPLE_POINT	1
		3	DDR_MODE1	1
		2	DDR_MODE0	1

Offset	Register name	Bits	Field name	Value
		1	BANDGAP_ENA1	1
		0	BANDGAP_ENA0	1
0x0E4	DIM_CA_IOC_CTLR_PNCNT_CFG	31:0	–	0x00001010
		31:13	Reserved	0
		12:8	NCNT_INIT_CSR	16
		7:5	Reserved	0
		4:0	PCNT_INIT_CSR	16
0x0E8	DIM_CA_IOC_CTLR_TIMER_CFG	31:0	–	0xFA000020
		31:16	TIMER_PERIOD	64000
		15:0	FF_TIMER_PERIOD	32
0x0F0	DIM_CA_IOC_CTLR_CHAR_CFG	31:0	–	0x00000000
		31:17	Reserved	0
		16	SM_BYP_ENA	0
		15	SM_BYP_N_ENA	0
		14:13	Reserved	0
		12:8	SM_BYP_NCNT	0
		7	SM_BYP_P_ENA	0
		6:5	Reserved	0
		4:0	SM_BYP_PCNT	0
0x100	DIM_CA_CA_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0

Offset	Register name	Bits	Field name	Value
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x110	DIM_CA_CK_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x100	DIM_DQ_DQ_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0

Offset	Register name	Bits	Field name	Value
		4:0	PCNT_SW_OFFSET	0
0x110	DIM_DQ_DQS_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x0	DIM_CA_TOP_CFG	31:0	–	0x00000031
		31:21	Reserved	0
		20	IOCAL_CTRL_SEL	0
		19:17	Reserved	0
		16	SDR_MODE_EN	0
		15:14	Reserved	0
		13	DEBUG_BUS_SEL	0
		12	DEBUG_BUS_EN	0
		11:9	Reserved	0
		8	CDC_TEST_EN	0
		7:6	Reserved	0
		5	WR_PIPE_EXTEND1	1
		4	WR_PIPE_EXTEND0	1
		3:1	Reserved	0

Offset	Register name	Bits	Field name	Value
		0	WR_CLK_SEL	1
0x4	DIM_CA_HW_INFO	31:0	–	0x00013007
		31:20	Reserved	0
		19:16	CORE_ID	1
		15:12	MAJOR_REV	3
		11:8	BRANCH_REV	0
		7:0	MINOR_REV	7
0x10	DIM_CA_PAD_CFG0	31:0	–	0x20222240
		31	CA_DDR_MODE1	0
		30	CA_DDR_MODE0	0
		29	CA_LV_MODE	1
		28	CA_ODT_ENA	0
		27:26	CA_ODT	0
		25:24	CA_PULL	0
		23:22	Reserved	0
		21:20	CA_NSLEW	2
		19:18	Reserved	0
		17:16	CA_PSLEW	2
		15:14	Reserved	0
		13:12	CA_NRXDEL	2
		11:10	Reserved	0
		9:8	CA_PRXDEL	2
		7	CA_VM_SHIFT_ENA	0
		6:4	CA_ROUT	4
		3	Reserved	0
		2:0	CA_DCC	0

Offset	Register name	Bits	Field name	Value
0x14	DIM_CA_PAD_CFG1	31:0	–	0x20220450
		31	CK_DDR_MODE1	0
		30	CK_DDR_MODE0	0
		29	CK_LV_MODE	1
		28	CK_CMFB_ENA	0
		27	CK_ODT_ENA1	0
		26	CK_ODT_ENA	0
		25:24	CK_ODT	0
		23:22	Reserved	0
		21:20	CK_NSLEW	2
		19:18	Reserved	0
		17:16	CK_PSLEW	2
		15:14	Reserved	0
		13	CK_CUR_MODE1	0
		12	CK_CUR_MODE0	0
		11	Reserved	0
		10:8	CK_I_DRV	4
		7	CK_VM_SHIFT_ENA	0
		6:4	CK_ROUT	5
		3	Reserved	0
		2:0	CK_DCC	0
0x18	DIM_CA_PAD_CFG2	31:0	–	0x10000000
		31:30	Reserved	0
		29	VREF_LDO_ENA	0
		28	VREF_PASSGATE_ENA	1
		27:24	VREF_SP_OUT	0
		23:22	Reserved	0

Offset	Register name	Bits	Field name	Value
		21:18	VREF_SP_IN	0
		17	VREF_BYPASS_ENA	0
		16	VREF_RDIV_ENA	0
		15:14	Reserved	0
		13:8	VREF_PULLDN_SPEED_CNTL	0
		7:6	Reserved	0
		5:0	VREF_LEVEL_CNT	0
0x1C	DIM_CA_PAD_CFG3	31:0	–	0x313003FF
		31:30	CS_N_IE	0
		29:28	CS_N_OE	3
		27:26	Reserved	0
		25	CK_IE	0
		24	CK_OE	1
		23:22	CKE_IE	0
		21:20	CKE_OE	3
		19:10	CA_IE	0
		9:0	CA_OE	1023
0x20	DIM_CA_PAD_CFG4	31:0	–	0x303003FF
		31:30	CS_N_OE_DYN_ENA	0
		29:28	CS_N_OE_DYN	3
		27:24	Reserved	0
		23:22	CKE_OE_DYN_ENA	0
		21:20	CKE_OE_DYN	3
		19:10	CA_OE_DYN_ENA	0
		9:0	CA_OE_DYN	1023

Offset	Register name	Bits	Field name	Value
0x0	DIM_DQ_TOP_CFG	31:0	–	0x00000031
		31:27	Reserved	0
		26	CDC_LDO_EN	0
		25	CDC_SWITCH_RC_EN	0
		24	CDC_SWITCH_BYPASS_OFF	0
		23:21	Reserved	0
		20	IOCAL_CTRL_SEL	0
		19:17	Reserved	0
		16	RCW_EN	0
		15:14	Reserved	0
		13	DEBUG_BUS_SEL	0
		12	DEBUG_BUS_EN	0
		11:9	Reserved	0
		8	CDC_TEST_EN	0
		7:6	Reserved	0
		5	WR_PIPE_EXTEND1	1
		4	WR_PIPE_EXTEND0	1
		3:1	Reserved	0
		0	WR_CLK_SEL	1
0x4	DIM_DQ_HW_INFO	31:0	–	0x00013007
		31:20	Reserved	0
		19:16	CORE_ID	1
		15:12	MAJOR_REV	3
		11:8	BRANCH_REV	0
		7:0	MINOR_REV	7

Offset	Register name	Bits	Field name	Value
0x10	DIM_DQ_PAD_CFG0	31:0	–	0xA0222250
		31	DQ_DDR_MODE1	1
		30	DQ_DDR_MODE0	0
		29	DQ_LV_MODE	1
		28	DQ_ODT_ENA	0
		27:26	DQ_ODT	0
		25:24	DQ_PULL	0
		23:22	Reserved	0
		21:20	DQ_NSLEW	2
		19:18	Reserved	0
		17:16	DQ_PSLEW	2
		15:14	Reserved	0
		13:12	DQ_NRXDEL	2
		11:10	Reserved	0
		9:8	DQ_PRXDEL	2
		7	DQ_VM_SHIFT_ENA	0
		6:4	DQ_ROUT	5
		3	Reserved	0
		2:0	DQ_DCC	0
0x14	DIM_DQ_PAD_CFG1	31:0	–	0xA0222250
		31	DQS_DDR_MODE1	1
		30	DQS_DDR_MODE0	0
		29	DQS_LV_MODE	1
		28	DQS_ODT_ENA	0
		27:26	DQS_ODT	0
		25:24	DQS_PULL	0
		23:22	Reserved	0

Offset	Register name	Bits	Field name	Value
		21:20	DQS_NSLEW	2
		19:18	Reserved	0
		17:16	DQS_PSLEW	2
		15:14	Reserved	0
		13:12	DQS_NRXDEL	2
		11:10	Reserved	0
		9:8	DQS_PRXDEL	2
		7	DQS_VM_SHIFT_ENA	0
		6:4	DQS_ROUT	5
		3	Reserved	0
		2:0	DQS_DCC	0
0x18	DIM_DQ_PAD_CFG2	31:0	–	0x10000000
		31:30	Reserved	0
		29	VREF_LDO_ENA	0
		28	VREF_PASSGATE_ENA	1
		27:24	VREF_SP_OUT	0
		23:22	Reserved	0
		21:18	VREF_SP_IN	0
		17	VREF_BYPASS_ENA	0
		16	VREF_RDIV_ENA	0
		15:14	Reserved	0
		13:8	VREF_PULLDN_SPEED_CNTL	0
		7:6	Reserved	0
		5:0	VREF_LEVEL_CNT	0
0x20	DIM_DQ_PAD_CFG3	31:0	–	0x1000FF11
		31:29	Reserved	0
		28	DQS_DIFF_MODE	1

Offset	Register name	Bits	Field name	Value
		27	RCW_ODT_ENA1	0
		26	RCW_ODT_ENA0	0
		25:24	RCW_ODT	0
		23	DQ_ODT_ENA1	0
		22	DQ_ODT_ENA0	0
		21:20	DQ_ODT	0
		19	DQS_ODT_ENA1	0
		18	DQS_ODT_ENA0	0
		17:16	DQS_ODT	0
		15:8	DQ_IE_OE	255
		7:6	Reserved	0
		5	RCW_IE_OE	0
		4	DQS_IE_OE	1
		3:2	Reserved	0
		1	DM_IE	0
		0	DM_OE	1
0x24	DIM_DQ_PAD_CFG4	31:0	–	0x20222250
		31	RCW_DDR_MODE1	0
		30	RCW_DDR_MODE0	0
		29	RCW_LV_MODE	1
		28:26	Reserved	0
		25:24	RCW_PULL_B	0
		23:22	Reserved	0
		21:20	RCW_NSLEW	2
		19:18	Reserved	0
		17:16	RCW_PSLEW	2
		15:14	Reserved	0

Offset	Register name	Bits	Field name	Value
		13:12	RCW_NRXDEL	2
		11:10	Reserved	0
		9:8	RCW_PRXDEL	2
		7	RCW_VM_SHIFT_ENA	0
		6:4	RCW_ROUT	5
		3	Reserved	0
		2:0	RCW_DCC	0
0x034	DIM_CA_CDC_CTLR_CFG1	31:0	–	0x3711111
		26:24	OSC_COUNT_DELAY	3
		22:20	STANDBY_DELAY	7
		18:16	DEL_MODE_DELAY	1
		14:12	OSC_MODE_DELAY	1
		10:8	DECODER_DELAY	1
		6:4	DIVIDER_DELAY	1
		2:0	MULTIPLIER_DELAY	1
0x038	DIM_CA_CDC_CAL_TIMER_CFG0	31:0	–	0x01201000
		24	INVALID_TIMER_ENA	1
		23:20	INVALID_TIMER_VAL	2
		16	TIMER_ENA	0
		15:0	TIMER_VAL	1000
0x03C	DIM_CA_CDC_CAL_TIMER_CFG1	31:0	–	0x00000006
		12	FF_TIMER_ENA	0
		9:0	FF_TIMER_VAL	6
0x040	DIM_CA_CDC_REFCOUNT_CFG	31:0	–	0x90AD2020
		31:16	TREF	90AD
		13:8	CCAL_REF_COUNT	20
		5:0	FCAL_REF_COUNT	20

Offset	Register name	Bits	Field name	Value
0x04C	DIM_CA_CDC_OFFSET_CFG	31:0	–	0x00000000
		20	SUBUNIT_OFFSET_MODE	0
		19	SUBUNIT_OFFSET_SIGN	0
		16:12	SUBUNIT_OFFSET	0
		8	UNIT_OFFSET_MODE	0
		7	UNIT_OFFSET_SIGN	0
		5:0	UNIT_OFFSET	0
0x050	DIM_CA_CDC_DELAY_CFG	31:0	–	0x00001D5
		28	TARGET_COUNT_ENA	0
		27:16	TARGET_COUNT	0
		11:0	DELAY_VAL	1D5
0x054	DIM_CA_CDC_SW_MODE_CFG	31:0	–	0x0
		3	SW_DEL_MODE	0
		2	SW_OSC_MODE	0
		1	SW_DA_SEL	0
		0	SW_LOAD	0
0x05C	DIM_CA_CDC_SW_OVRD_CFG	31:0	–	0x00000000
		16	SW_REF_GATE	0
		11	SW_OVRD_DA1_OSC_EN	0
		10	SW_OVRD_DA1_IN_EN	0
		9	SW_OVRD_DA0_OSC_EN	0
		8	SW_OVRD_DA0_IN_EN	0
		3	SW_OVRD_CDC_COUNTER_RST	0
		2	SW_OVRD_LOAD_DA_SEL	0
		1	SW_OVRD_ACTV_DA_SEL	0
		0	SW_OVRD_ENA	0

Offset	Register name	Bits	Field name	Value
0x034	DIM_DQ_CDC_CTLR_CFG1	31:0	–	0x03011111
		26:24	OSC_COUNT_DELAY	3
		22:20	STANDBY_DELAY	0
		18:16	DEL_MODE_DELAY	1
		14:12	OSC_MODE_DELAY	1
		10:8	DECODER_DELAY	1
		6:4	DIVIDER_DELAY	1
		2:0	MULTIPLIER_DELAY	1
0x038	DIM_DQ_CDC_CAL_TIMER_CFG0	31:0	–	0x01201000
		24	INVALID_TIMER_ENA	1
		23:20	INVALID_TIMER_VAL	2
		16	TIMER_ENA	0
		15:0	TIMER_VAL	1000
0x03C	DIM_DQ_CDC_CAL_TIMER_CFG1	31:0	–	0x00060000
		12	FF_TIMER_ENA	0
		9:0	FF_TIMER_VAL	6
0x040	DIM_DQ_CDC_REFCOUNT_CFG	31:0	–	0x90AD2020
		31:16	TREF	90AD
		13:8	CCAL_REF_COUNT	20
		5:0	FCAL_REF_COUNT	20
0x04C	DIM_DQ_RD_CDC_OFFSET_CFG	31:0	–	0x00000000
		20	SUBUNIT_OFFSET_MODE	0
		19	SUBUNIT_OFFSET_SIGN	0
		16:12	SUBUNIT_OFFSET	0
		8	UNIT_OFFSET_MODE	0
		7	UNIT_OFFSET_SIGN	0
		5:0	UNIT_OFFSET	0

Offset	Register name	Bits	Field name	Value
0x050	DIM_DQ_RD_CDC_DELAY_CFG	31:0	–	0x000001D5
		28	TARGET_COUNT_ENA	0
		27:16	TARGET_COUNT	0
		11:0	DELAY_VAL	1D5
0x054	DIM_DQ_RD_CDC_SW_MODE_CFG	31:0	–	0x00000000
		3	SW_DEL_MODE	0
		2	SW_OSC_MODE	0
		1	SW_DA_SEL	0
		0	SW_LOAD	0
0x05C	DIM_DQ_RD_CDC_SW_OVRD_CFG	31:0	–	0x00000000
		16	SW_REF_GATE	0
		11	SW_OVRD_DA1_OSC_EN	0
		10	SW_OVRD_DA1_IN_EN	0
		9	SW_OVRD_DA0_OSC_EN	0
		8	SW_OVRD_DA0_IN_EN	0
		3	SW_OVRD_CDC_COUNTER_RST	0
		2	SW_OVRD_LOAD_DA_SEL	0
		1	SW_OVRD_ACTV_DA_SEL	0
		0	SW_OVRD_ENA	0
0x060	DIM_DQ_RD_CDC_SLAVE_DDA_CFG	31:0	–	0x0001626C
		17	SLAV_DDA_OFFSET_MODE	0
		16	SLAV_DDA_OFFSET_SIGN	1
		15:12	SLAVE_DDA_OFFSET	6
		10:0	SLAVE_DDA_DELAY	26C

Offset	Register name	Bits	Field name	Value
0x0AC	DIM_DQ_WR_CDC_OFFSET_CFG	31:0	–	0x00000000
		20	SUBUNIT_OFFSET_MODE	0
		19	SUBUNIT_OFFSET_SIGN	0
		16:12	SUBUNIT_OFFSET	0
		8	UNIT_OFFSET_MODE	0
		7	UNIT_OFFSET_SIGN	0
		5:0	UNIT_OFFSET	0
0x0B0	DIM_DQ_WR_CDC_DELAY_CFG	31	–	0x0000001D5
		28	TARGET_COUNT_ENA	0
		27:16	TARGET_COUNT	0
		11:0	DELAY_VAL	1D5
0x0B4	DIM_DQ_WR_CDC_SW_MODE_CFG	31	–	0
		3	SW_DEL_MODE	0
		2	SW_OSC_MODE	0
		1	SW_DA_SEL	0
		0	SW_LOAD	0
0x0BC	DIM_DQ_WR_CDC_SW_OVRD_CFG	31	–	0x00000000
		16	SW_REF_GATE	0
		11	SW_OVRD_DA1_OSC_EN	0
		10	SW_OVRD_DA1_IN_EN	0
		9	SW_OVRD_DA0_OSC_EN	0
		8	SW_OVRD_DA0_IN_EN	0
		3	SW_OVRD_CDC_COUNTER_RST	0
		2	SW_OVRD_LOAD_DA_SEL	0
		1	SW_OVRD_ACTV_DA_SEL	0
		0	SW_OVRD_ENA	0

2.1.4 Recommended settings for clock frequency-dependent APQ8064E registers

Certain register settings depend on the APQ8064E clock frequency. This section lists these clock frequency-dependent registers. Table 2-3 lists these register settings for the EBI bus clock frequency of 533 MHz.

Table 2-3 Clock frequency-dependent register settings for EBI0/EBI1 at 533 MHz

Offset	Register name	Bits	Field name	Value
0x80058	DDR_DRAM_TIMING_0	31:0	–	0x5BA06017
		31:29	TRTP	2
		28:24	TFAW	27
		23:20	TRCD	10
		19:16	Reserved	0
		15:12	TRRD	6
		11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	0
		8:7	Reserved	0
		6:5	tZQCL_MSB	0
		4:0	TRAS_MIN	23
0x8005C	DDR_DRAM_TIMING_1	31:0	–	0x00044825
		31:30	Reserved	0
		29	INCL_DARF_MAX_NUM_ACT_RANK1	0
		28	INCL_DARF_MAX_NUM_ACT_RANK0	0
		27:20	Reserved	0
		19:16	MAX_NUM_ACT_RANK1	4
		15:12	MAX_NUM_ACT_RANK0	4
		11:8	MAX_NUM_REFRESHES_TREFBW	8
		7	Reserved	0
		6:4	TMRD_READS	2
		3	Reserved	0
		2:0	TMRD_WRITES	5

Offset	Register name	Bits	Field name	Value
0x80060	DDR_DRAM_TIMING_2	31:0	–	0xE18C0220
		31:21	TRAS_MAX	1804
		20:18	TCKE	3
		17:15	Reserved	0
		14:12	WR_TO_RD_DLY_DIFF_RANK	0
		11	Reserved	0
		10:8	TRTW_SAME_RANK	2
		7	Reserved	0
		6:4	TRTW_DIFF_RANK	2
		3	Reserved	0
		2:0	TOST	0
0x80064	DDR_DRAM_TIMING_3	31:0	–	0x0440964B
		31:28	PD_EXIT_DURATION_ODT	0
		27:24	TWTR	4
		23	PD_EXIT_DURATION_ODT_MSB	0
		22:19	TWR	8
		18:9	TXSRD	75
		8	Reserved	0
		7:0	TXSNR	75
0x80068	DDR_DRAM_TIMING_4	31:0	–	0x46044440
		31:24	TRFC	70
		23:20	TMOD	0
		19:16	TXPNR_ACT_PWR_DOWN	4
		15:12	TXPR_ACT_PWR_DOWN	4
		11:8	TXPNR_PCHG_PWR_DOWN	4
		7:4	TXPR_PCHG_PWR_DOWN	4
		3:2	Reserved	0

Offset	Register name	Bits	Field name	Value
		1	TXPNR_PCHG_PWR_DOWN_MSB	0
		0	TXPR_PCHG_PWR_DOWN_MSB	0
0x8006C	DDR_DRAM_TIMING_5	31:0	–	0x0812C0AB
		31:24	SELF_RFSH_MIN_DURATION	8
		23	Reserved	0
		22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	1
		19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	2
		15:12	TRP_AB	12
		11:8	CLK_RESTART_BEFORE_SR_EXIT_UPPER	0
		7:4	TRP_PB	10
		3:0	RD_LATENCY	11
0x80070	DDR_DRAM_TIMING_6	31:0	–	0x50212000
		31:28	WR_LATENCY	5
		27:24	Reserved	0
		23:20	RESTART_CLK_PWR_DOWN_EXIT	2
		19	Reserved	0
		18:16	STOP_CLK_PWR_DOWN_ENTRY	1
		15:14	Reserved	0
		13:12	TSRR	2
		11:8	Reserved	0
		7:4	Reserved	0
		3:0	Reserved	0
0x80074	DDR_DRAM_TIMING_7	31:0	–	0xC0611F83
		31:24	TZQCL	192
		23:17	TZQCS	48
		16	PAD_LOW_POWER_MODE	1

Offset	Register name	Bits	Field name	Value
		15:12	DLY_RD_CAPTURE	1
		11:8	EXT_RD_CAPTURE	15
		7:4	DLY_IE_START	8
		3:0	EXT_IE_WINDOW	3
0x80078	DDR_DRAM_TIMING_8	31:0	–	0x01010101
		31:30	Reserved	0
		29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	0
		27:24	RCW_START_DLY_BYTE3	1
		23:22	Reserved	0
		21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	0
		19:16	RCW_START_DLY_BYTE2	1
		15:14	Reserved	0
		13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	0
		11:8	RCW_START_DLY_BYTE1	1
		7:6	Reserved	0
		5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	0
		3:0	RCW_START_DLY_BYTE0	1
0x8007C	DDR_DRAM_TIMING_9	31:0	–	0x00000000
		31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	0
		23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	0
		15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	0
		7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	0
0x80080	DDR_DRAM_TIMING_0_ALT	31:0	–	0x5BA0617
		31:29	TRTP	2
		28:24	TFAW	27
		23:20	TRCD	10
		19:16	Reserved	0

Offset	Register name	Bits	Field name	Value
		15:12	TRRD	6
		11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	0
		8:7	Reserved	0
		6:5	tZQCL_MSB	0
		4:0	TRAS_MIN	23
0x80084	DDR_DRAM_TIMING_3_ALT	31:0	–	0x0440964B
		31:28	PD_EXIT_DURATION_ODT	0
		27:24	TWTR	4
		23	PD_EXIT_DURATION_ODT_MSB	0
		22:19	TWR	8
		18:9	TXSRD	75
		8	Reserved	0
		7:0	TXSNR	75
0x80088	DDR_DRAM_TIMING_4_ALT	31:0	–	0x46044440
		31:24	TRFC	70
		23:20	TMOD	0
		19:16	TXPNR_ACT_PWR_DOWN	4
		15:12	TXPR_ACT_PWR_DOWN	4
		11:8	TXPNR_PCHG_PWR_DOWN	4
		7:4	TXPR_PCHG_PWR_DOWN	4
		3:2	Reserved	0
		1	TXPNR_PCHG_PWR_DOWN_MSB	0
		0	TXPR_PCHG_PWR_DOWN_MSB	0
0x8008C	DDR_DRAM_TIMING_5_ALT	31:0	–	0x0812C0AB
		31:24	SELF_RFSH_MIN_DURATION	8
		23	Reserved	0
		22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	1

Offset	Register name	Bits	Field name	Value
		19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	2
		15:12	TRP_AB	12
		11:8	Reserved	0
		7:4	TRP_PB	10
		3:0	RD_LATENCY	11
0x80090	DDR_DRAM_TIMING_7_ALT	31:0	–	0xC0611F83
		31:24	TZQCL	192
		23:17	TZQCS	48
		16	PAD_LOW_POWER_MODE	1
		15:12	DLY_RD_CAPTURE	1
		11:8	EXT_RD_CAPTURE	15
		7:4	DLY_IE_START	8
		3:0	EXT_IE_WINDOW	3
0x80094	DDR_DRAM_TIMING_8_ALT	31:0	–	0x01010101
		31:30	Reserved	0
		29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	0
		27:24	RCW_START_DLY_BYTE3	1
		23:22	Reserved	0
		21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	0
		19:16	RCW_START_DLY_BYTE2	1
		15:14	Reserved	0
		13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	0
		11:8	RCW_START_DLY_BYTE1	1
		7:6	Reserved	0
		5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	0
		3:0	RCW_START_DLY_BYTE0	1

Offset	Register name	Bits	Field name	Value
0x80098	DDR_DRAM_TIMING_9_ALT	31:0	–	0x00000000
		31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	0
		23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	0
		15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	0
		7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	0
0x8009C	DDR_UPDATE_FREQ_CHANGE_ALT	31:0	–	0x50000000
		31:28	WR_LATENCY	5
		27:22	Reserved	0
		21:19	ODT_START_DELAY_WR	0
		18:16	ODT_START_DELAY_RD	0
		15:13	ODT_OFF_DELAY	0
		12:4	Reserved	0
		3:1	tANPD	0
		0	Reserved	0

2.2 APQ8064E EBI0/EBI1 register settings for PCDDR3

The recommended settings in this document are intended to support the APQ8064E with the 533 MHz PCDDR3 SDRAM clock frequency.

2.2.1 Device characteristics

Table 2-4 lists the key device characteristics required to set up the EBI0/EBI1 registers. The values supply information (for example, clock speed), temperature parameters, and organization parameters. Refer to the device's datasheet for more details on how to adjust the device settings based on the characteristics.

Table 2-4 EBI0/EBI1 PCDDR3 SDRAM interface information

Parameter	Value	Unit
DDR_CLK freq	533	MHz
XO freq	27	MHz
Sleep_CLK_Freq	32	kHz

Parameter	Value	Unit
DDR SDRAM device parameters		
tRP	13.1	ns
tWR	15	ns
tRRD	10	ns
tWTR	7.5	ns
tXP	7.5	ns
tXPDLL (if available)	24	ns
tXS (if available)	120	ns
tCKE	5.625	ns
tRFC	110	ns
tRCD	13.1	ns
tRAS	37.5 (min.)	ns
	70200 (max.)	ns
tRC	50.625	ns
tFAW	50	ns
tRTP	7.5	ns
WL	6	tCK
RL	7	tCK
AL	0	
CL	7	
CWL	6	
tDQSCK	-0.3 (min.)	ns
	0.3 (max.)	ns
tREFI	7.8	µs
tMRD	4	tCK
tZQoper	320	ns
tZQCS	80	ns

Parameter	Value	Unit
tZQINIT	640	ns
tMOD	15	ns
tCKSRE	10	ns
tCKSRX	10	ns
tCKESR	tCKE + 1	tCK
tDQSQ	0.15	ns
tHZ(DQ)	–	ns
	0.3 (max.)	
tLZ(DQ)	-0.6 (min.)	ns
	0.3 (max.)	ns
ODTH8	6	tCK
TXSDLL	512	tCK
tAOFPD	2 (min.)	ns
	8.5 (max.)	ns
Number of rows (CS0)	16384	
Number of columns (CS0)	1024	
Number of banks (CS0)	8	
Number of rows (CS1)	16384	
Number of columns (CS1)	1024	
Number of banks (CS1)	8	
Number of required refreshes R	8192	
Burst length	8	
Device density (CS0)	512	
Device density (CS1)	512	

NOTE: All the specifications listed in Table 2-4 are based on the Micron MT41J128M16HA-15E:D device. Mobile designers are responsible for using appropriate specification values corresponding to the PCDDR3 devices of interest.

2.2.2 Recommended settings for EBI0/EBI1 mode configuration

DDR_MR_CNTL_WDATA sets the SDRAM device into a specific mode. They also define device operation behaviors, e.g., burst length, drive strength, or partial refresh settings. Refer to the device manufacturer's data sheet for details about mode registers.

2.2.3 Recommended settings for APQ8064E registers

Table 2-5 provides recommended settings for clock frequency-independent registers.

Table 2-5 Clock frequency-independent registers

Offset	Register name	Bits	Field name	Value
0x00004	TOP_MISC_CNTL	31:0	–	0x0004F0EC
		31:21	Reserved	0
		20	IOCAL_UPDATE_METHOD	0
		19:16	IOCAL_UPDATE_PULSE_WIDTH	4
		15	CLKON_DDR_PIPE_MANUAL	1
		14	MODE_CLKON_DDR_PIPE	1
		13	CLKON_DDR_2X_MANUAL	1
		12	MODE_CLKON_DDR_2X	1
		11	MODE_MEM_HALT	1
		10:8	Reserved	0
		7	CLKON_AHB_MANUAL	1
		6	MODE_CLKON_AHB	1
		5	CLKON_DDR_1x_MANUAL	1
		4	MODE_CLKON_DDR_1x	0
		3	CLKON_AXI_MANUAL	1
		2	MODE_CLKON_AXI	1
		1:0	Reserved	0
0x40000	SLV_CONFIG	31:0	–	0x01001007
		31	CLKON_DISABLE	0
		30:26	Reserved	0

Offset	Register name	Bits	Field name	Value
		25:16	CLKON_IDLE_TIMER	256
		15:14	Reserved	0
		13:12	INTERLEAVE	1
		11:10	Reserved	0
		9:8	CMD_ORDERING	0
		7:3	Reserved	0
		2:0	CMD_Q_DEPTH	7
0x40004	SLV_RD_CONFIG	31:0	–	0x000B003F
		31:22	Reserved	0
		21:16	RD_CMD_FIFO_DEPTH	11
		15:6	Reserved	0
		5:0	RD_DATA_FIFO_DEPTH	63
0x40008	SLV_RD_STATUS (RD)	31:0	–	0x00000000
		31:28	Reserved	0
		27:24	RDQUAL_FIFO_ENTRIES_IN_USE	0
		23:16	RDDATA_FIFO_ENTRIES_IN_USE	0
		15:8	RDDATA_FIFO_EMPTY	0
		7:1	Reserved	0
		0	DQS_ERROR	0
0x4000C	SLV_WR_CONFIG	31:0	–	0xC708040F
		31	COALESCE_EN	1
		30	READ_MERGE_EN	1
		29	FLUSH	0
		28	EMPTY	0
		27	WRITE_BLOCK_READ	0
		26:24	CMD_BUF_DEPTH	7
		23:21	Reserved	0

Offset	Register name	Bits	Field name	Value
		20:16	FLUSH_UPPER_LIMIT	8
		15:13	Reserved	0
		12:8	FLUSH_LOWER_LIMIT	4
		7:5	Reserved	0
		4:0	WR_BUFFER_DEPTH	15
0x40010	SLV_FLUSH_CONFIG	31:0	–	0x00008010
		31:30	FLUSH_PRIORITY	0
		29	Reserved	0
		28	FLUSH_IN_ORDER	0
		27:18	Reserved	0
		17:8	FLUSH_IDLE_DELAY	128
		7:0	PAGE_HIT_WINDOW	16
0x40014	SLV_ID_REVISION (RD)	31:0	–	0x00005310
		31:16	Reserved	0
		15:12	REV_MAJOR	5
		11:08	REV_MINOR	3
		7:4	SITE_ID	1
		3:0	Reserved	0
0x40020	SLV_ADDR_BASE_CS0	31:0	–	0x00008000
		31:16	Reserved	–
		15:8	BASE_ADDR	128
		7:0	Reserved	0
0x40024	SLV_ADDR_BASE_CS1	31:0	–	0x0000C000
		31:16	Reserved	–
		15:8	BASE_ADDR	192
		7:0	Reserved	–

Offset	Register name	Bits	Field name	Value
0x40030	SLV_ADDR_MAP_CS0	31:0	–	0x00008122
		31:16	Reserved	0
		15	RANK_EN	1
		14	Reserved	0
		13:12	ADDR_MAP_MODE	0
		11:9	Reserved	0
		8	NUM_BANK	1
		7:6	Reserved	0
		5:4	WIDTH_ROW	2
		3:2	Reserved	0
		1:0	WIDTH_COL	2
0x40034	SLV_ADDR_MAP_CS1	31:0	–	0x00008122
		31:16	Reserved	0
		15	RANK_EN	1
		14	Reserved	0
		13:12	ADDR_MAP_MODE	0
		11:9	Reserved	0
		8	NUM_BANK	1
		7:6	Reserved	0
		5:4	WIDTH_ROW	2
		3:2	Reserved	0
		1:0	WIDTH_COL	2
0x40040	SLV_ADDR_SIZE_MASK_CS0	31:0	–	0x0000E000
		31:16	Reserved	0
		15:8	ADDR_MASK	224
		7:0	Reserved	0

Offset	Register name	Bits	Field name	Value
0x40044	SLV_ADDR_SIZE_MASK_CS1	31:0	–	0x0000E000
		31:16	Reserved	0
		15:8	ADDR_MASK	224
		7:0	Reserved	0
0x40050	SLV_STALL	31:0	–	0x00000004
		31:3	Reserved	0
		2	AXI_IDLE	1
		1	STALL_ACK	0
		0	STALL_REQ	0
0x40100	SLV_ERR_ADDR (RD)	31:0	–	0x00000000
		31:0	ERR_ADDR	0
0x40108	SLV_ERR_APACKET_0 (RD)	31:0	–	0x00000000
		31:16	Reserved	0
		15:0	ERR_AMID	0
0x4010C	SLV_ERR_APACKET_1 (RD)	31:0	–	0x00000000
		31:28	Reserved	0
		27:24	ERR_ALEN	0
		23:16	ERR_ATID	0
		15:13	ERR_ASIZE	0
		12	ERR_ABURST	0
		11:8	ERR_ATYPE	0
		7:6	ERR_ALOCK	0
		5:4	Reserved	0
		3	ERR_APROTNS	0
		2	ERR_AOOORD	0
		1	ERR_AOOOWR	0
		0	ERR_AWRITE	0

Offset	Register name	Bits	Field name	Value
0x40114	SLV_ERR_CNTL	31:0	–	0x00001000
		31:13	Reserved	0
		12	IRQ_EN	1
		11:9	Reserved	0
		8	CLEAR_ERR	0
		7:5	Reserved	0
		4	ERR_OCCURRED	0
		3:2	Reserved	0
		1:0	ERR_CODE	0
0x80000	DDR_DEVICE_CONFIG	31:0	–	0x0A004203
		31:28	Reserved	0
		27:26	DEVICE_CONFIG_RANK1	2
		25:24	DEVICE_CONFIG_RANK0	2
		23:18	Reserved	0
		17	INIT_DONE_RANK1	0
		16	INIT_DONE_RANK0	0
		15:14	NUM_BANKS	1
		13:12	Reserved	0
		11:10	CLK_SYNC_MODE	0
		9:7	DEVICE_TYPE	4
		6	Reserved	0
		5	MEM_CLK_CONFIG	0
		4	DDR_COMMAND_BUS	1
		3:2	Reserved	0
		1	RANK1_EN	1
		0	RANK0_EN	1

Offset	Register name	Bits	Field name	Value
0x80004	DDR_DEVICE_STATUS (RD)	31:0	–	0x00000000
		31:18	Reserved	0
		17	INTERRUPT_EN	0
		16	CURR_SEL_REG_FREQ_SWITCH	0
		15:14	Reserved	0
		13	IN_DEEP_POWER_DOWN_RANK1	0
		12	IN_DEEP_POWER_DOWN_RANK0	0
		11:10	Reserved	0
		9	IN_SELF_RFSH_RANK1	0
		8	IN_SELF_RFSH_RANK0	0
		7:6	Reserved	0
		5	RANK1_TEMP_OO_RANGE	0
		4	RANK0_TEMP_OO_RANGE	0
		3:2	Reserved	0
		1	RANK1_IDLE	0
		0	RANK0_IDLE	0
0x80010	DDR_MANUAL_CMD	31:0	–	0x00000000
		31:18	Reserved	0
		17:16	RANK_SEL	0
		15	Reserved	0
		14	CK_ON	0
		13	CKE	0
		12	RESET_N	0
		11:7	Reserved	0
		6	ENTER_DEEP_PD	0
		5	EXIT_DEEP_PD	0
		4	ZQ_CAL_SHORT	0

Offset	Register name	Bits	Field name	Value
		3	ZQ_CAL_LONG	0
		2	AUTO_REFRESH	0
		1	PRECHARGE_ALL	0
		0	SR_READ	0
0x80014	DDR_MR_CNTL_WDATA	31:0	–	0x00200000
		31:24	MR_ADDR	0
		23:20	Reserved	0
		22	RD_DQCAL	0
		21:20	RD_DQCAL_EXP_PATTERN	2
		19:18	MR_RANK_SEL	0
		17	MRR	0
		16	MRW	0
		15:0	MR_WDATA	0
0x80020	DDR_MR_RDATA_RANK0 (RD)	31:0	–	0x00000000
		31:0	MR_RDATA	0
0x80024	DDR_MR_RDATA_RANK1 (RD)	31:0	–	0x00000000
		31:0	MR_RDATA	0
0x80028	DDR_MRR_REPEAT	31:0	–	0x0000C000
		31:24	MRR_ADDR	0
		23:19	Reserved	0
		18:16	MRR_INTERVAL	0
		15:14	MRR_RANK_SEL	3
		13:12	Reserved	0
		11:8	MRR_INTERVAL_OVERRIDE	0
		7:0	Reserved	0

Offset	Register name	Bits	Field name	Value
0x80034	DDR_MRR_REPEAT_DATA_RANK0 (RD)	31:0	–	0x00000000
		31:0	MRR_DATA	0
0x80038	DDR_MRR_REPEAT_DATA_RANK1 (RD)	31:0	–	0x00000000
		31:0	MRR_DATA	0
0x8003C	DDR_CMD_EXEC_OPT_0	31:0	–	0x00208004
		31:28	Reserved	–
		27:16	PAGE_OPEN_TIMER	32
		15	PAGE_MGMT_POLICY	1
		14:7	RDCMD_STARVATION_TIMER	0
		6	WR_RD_PREF	0
		5	DDR_CK_ALWAYS_ON_DBG_MODE	0
		4	CONCURRENT_SELF_REFRESH_EN	0
		3	SEL_REG_FREQ_SWITCH	0
		2	PWR_DOWN_EN	1
		1	CLK_STOP_EN	0
		0	CLK_STOP_DURING_PWR_DOWN_EN	0
0x80040	DDR_CMD_EXEC_OPT_1	31:0	–	0x0000033B
		31:28	Reserved	0
		27	SELF_REFRESH_RANK1	0
		26	SELF_REFRESH_RANK0	0
		25:22	Reserved	0
		21:12	RANK_IDLE_TIMER	0
		11:8	RUN_ATLEAST_ONE_TRANS_RD_CONFLICT	3
		7:4	RUN_ATLEAST_ONE_TRANS_WR_CONFLICT	3
		3	ENABLE_DDR2X_CLKON_DURING_CSPD	1

Offset	Register name	Bits	Field name	Value
		2	ENABLE_POWER_OPT_AUTO_SRR_ZQ	0
		1	ENABLE_CMD_ADDR_OE_CNTL	1
		0	LOAD_TRP_CNTL	1
0x80044	DDR_CMD_EXEC_OPT_2	31:0	–	0x22040391
		31	Reserved	0
		30:28	ZQCAL_INTERVAL	2
		27:20	CLKON_IDLE_TIMER	32
		19:14	CLKON2X_ASSERT_WAIT_TIMER	16
		13:10	Reserved	0
		9:8	RDCMD_HP_REMAP_LEVEL3	3
		7:6	RDCMD_HP_REMAP_LEVEL2	2
		5:4	RDCMD_HP_REMAP_LEVEL1	1
		3:2	RDCMD_HP_REMAP_LEVEL0	0
		1:0	Reserved	0
		0	UPDATE_MEM_LATENCY_ON_FREQ_SWITCH	1
0x80048	DDR_CMD_EXEC_OPT_3	31:0	–	0x520B9B5B
		31	CODT_ON_WR	0
		30	CODT_ON_RD	0
		29	RANK1_ODT_ON_WR_RANK1	0
		28	RANK1_ODT_ON_WR_RANK0	0
		27	RANK1_ODT_ON_RD_RANK1	0
		26	RANK1_ODT_ON_RD_RANK0	0
		25	RANK0_ODT_ON_WR_RANK1	0
		24	RANK0_ODT_ON_WR_RANK0	0
		23	RANK0_ODT_ON_RD_RANK1	0
		22	RANK0_ODT_ON_RD_RANK0	0

Offset	Register name	Bits	Field name	Value
		21:19	ODT_START_DELAY_WR	1
		18:16	ODT_START_DELAY_RD	3
		15:13	ODT_OFF_DELAY	4
		12:10	ODTH8	6
		9	EN_ODT_SWITCH_RANK_UNAVAIL	1
		8	EN_ODT_POWER_DOWN	1
		7:6	ODT_EXTEND_DELAY_WR	1
		5:4	ODT_EXTEND_DELAY_RD	1
		3:1	tANPD	5
		0	DLL_CNTL_PCHG_PD	1
0x8004C	DDR_CMD_EXEC_OPT_4	31:0	–	0x20000000
		31: 24	PWR_DOWN_IDLE_TIMER	32
		23:0	Reserved	0
0x80050	DDR_SM_TIMING_0	31:0	0x0000.0004 (reset default)	0x00001084
		31:15	Reserved	0
		14:12	DLY_RD_DIFF_RANK	1
		11	RD_INT_BY_RD	0
		10	WR_INT_BY_WR	0
		9	RD_INT_BY_BST	0
		8	WR_INT_BY_BST	0
		7:6	WR_INT_RD_OR_PRECHG_MODE	2
		5:4	Reserved	0
		3:2	INT_BOUNDARY	1
		1:0	Reserved	0
0x80054	DDR_SM_TIMING_1	31:0	–	0x003F00B4
		31:24	Reserved	0
		23:20	MEM_START_BURST_RD	3

Offset	Register name	Bits	Field name	Value
		19:16	MEM_START_BURST_WR	15
		15:14	SYS_TIMING_MODE	0
		13:8	Reserved	0
		7	USE_ORIG_BL	1
		6	Reserved	0
		5	ON_THE_FLY_MODE	1
		4	DRIVE_WR_DQS_EARLY	1
		3:0	BURST_LENGTH	4
0x800A0	DDR_AUTO_RFSH_CNTL	31:0	–	0x07345007
		31:28	Reserved	0
		27:24	COUNT_RFSH_AHEAD	7
		23	TEMP_ADJUST_RFSH	0
		22:14	TREFI	209
		13:12	MODE_AUTO_RFSH	1
		11:3	Reserved	0
		2:0	REFRESH_IDLE_ACROSS_RANKS	7
0x800A8	DDR_SELF_RFSH_CNTL	31:0	–	0x0C002000
		31:28	Reserved	0
		27	HW_SELF_RFSH_EN_RANK1	1
		26	HW_SELF_RFSH_EN_RANK0	1
		25:20	Reserved	0
		19:8	HW_SELF_RFSH_TIMER	32
		7:0	Reserved	0
0x80200	DDR_ENHPRI_EN	31:0	–	0xED900000
		31	ENHANCED_PRI_EN	1
		30	RD_PRI_AGING_EN	1
		29	WR_PRI_AGING_EN	1

Offset	Register name	Bits	Field name	Value
		28	Reserved	0
		27	ADJ_PRI_RDBLOCKING	1
		26	ADJ_PRI_RDMERGE	1
		25:24	PRI_RDBLOCKING	1
		23	ADJ_PRI_WRBLOCKING	1
		22	Reserved	0
		21:20	PRI_WRBLOCKING	1
		19:16	Reserved	0
		15:8	CONFLICT_BLOCK_HIT	0
		7	Reserved	0
0x80224	DDR_ENHPRI_RD1	31:0	–	0x00000008
		31:7	Reserved	0
		6:0	CYCLES_AXIPRI0	8
0x80228	DDR_ENHPRI_RD2	31:0	–	0x00000000
		31:7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x8022C	DDR_ENHPRI_RD3	31:0	–	0x00000800
		31:15	Reserved	0
		14:8	CYCLES_AXIPRI1	8
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80230	DDR_ENHPRI_RD4	31:0	–	0x00004040
		31:15	Reserved	0
		14:8	CYCLES_AXIPRI1	64
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	64

Offset	Register name	Bits	Field name	Value
0x80234	DDR_ENHPRI_RD5	31:0	–	0x00000000
		31:23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80238	DDR_ENHPRI_RD6	31:0	–	0x00000000
		31:23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x8023C	DDR_ENHPRI_RD7	31:0	–	0x00000000
		31	Reserved	0
		30:24	CYCLES_AXIPRI3	0
		23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	0
0x80248	DDR_ENHPRI_WR2	31:0	–	0x00000000
		31:7	Reserved	0
		6:0	CYCLES_AXIPRI0	0

Offset	Register name	Bits	Field name	Value
0x80250	DDR_ENHPRI_WR4	31:0	–	0x00000040
		31:15	Reserved	0
		14:8	CYCLES_AXIPRI1	0
		7	Reserved	0
		6:0	CYCLES_AXIPRI0	64
0x80258	DDR_ENHPRI_WR6	31:0	–	0x00000000
		31:23	Reserved	0
		22:16	CYCLES_AXIPRI2	0
		15	Reserved	–
		14:8	CYCLES_AXIPRI1	–
		7	Reserved	–
		6:0	CYCLES_AXIPRI0	0
0x0E0	DIM_CA_IOC_CTLR_CFG	31:0	–	0x4101071F
		31	CAL_NOW	0
		30	IO_CAL_AUTO	1
		29	IO_CAL_FF_TIMER_EN	0
		28	IO_CAL_BANDGAP_DYN_CTRL	0
		27:26	Reserved	0
		25	SW_FFCLK_ON	0
		24	LV_MODE	1
		23:21	Reserved	0
		20:16	MARGIN_LOAD	1
		15:14	Reserved	0
		13:12	IMP_SEL	0
		11	Reserved	0
		10	PN_SEL_CA	1
		9	PN_SEL_DATA	1

Offset	Register name	Bits	Field name	Value
		8	CAL_USE_LAST	1
		7	Reserved	0
		6:4	SAMPLE_POINT	1
		3	DDR_MODE1	1
		2	DDR_MODE0	1
		1	BANDGAP_ENA1	1
		0	BANDGAP_ENA0	1
0x0E4	DIM_CA_IOC_CTLR_PNCNT_CFG	31:0	–	0x00001010
		31:13	Reserved	0
		12:8	NCNT_INIT_CSR	16
		7:5	Reserved	0
		4:0	PCNT_INIT_CSR	16
0x0E8	DIM_CA_IOC_CTLR_TIMER_CFG	31:0	–	0xFA000020
		31:16	TIMER_PERIOD	64000
		15:0	FF_TIMER_PERIOD	32
0x0F0	DIM_CA_IOC_CTLR_CHAR_CFG	31:0	–	0x00000000
		31:17	Reserved	0
		16	SM_BYP_ENA	0
		15	SM_BYP_N_ENA	0
		14:13	Reserved	0
		12:8	SM_BYP_NCNT	0
		7	SM_BYP_P_ENA	0
		6:5	Reserved	0
		4:0	SM_BYP_PCNT	0
0x100	DIM_CA_CA_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0

Offset	Register name	Bits	Field name	Value
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x110	DIM_CA_CK_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x100	DIM_DQ_DQ_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0

Offset	Register name	Bits	Field name	Value
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x110	DIM_DQ_DQS_IOC_SLV_CFG	31:0	–	0x80000000
		31	PNCNT_HW_LOAD_EN	1
		30:29	Reserved	0
		28:24	NCNT_SW_VAL	0
		23:21	Reserved	0
		20:16	PCNT_SW_VAL	0
		15	NCNT_OFFSET_SIGN	0
		14:13	Reserved	0
		12:8	NCNT_SW_OFFSET	0
		7	PCNT_OFFSET_SIGN	0
		6:5	Reserved	0
		4:0	PCNT_SW_OFFSET	0
0x0	DIM_CA_TOP_CFG	31:0	–	0x00010031
		31:21	Reserved	0
		20	IOCAL_CTRL_SEL	0
		19:17	Reserved	0
		16	SDR_MODE_EN	1
		15:14	Reserved	0
		13	DEBUG_BUS_SEL	0
		12	DEBUG_BUS_EN	0
		11:9	Reserved	0

Offset	Register name	Bits	Field name	Value
		8	CDC_TEST_EN	0
		7:6	Reserved	0
		5	WR_PIPE_EXTEND1	1
		4	WR_PIPE_EXTEND0	1
		3:1	Reserved	0
		0	WR_CLK_SEL	1
0x4	DIM_CA_HW_INFO	31:0	–	0x00013007
		31:20	Reserved	0
		19:16	CORE_ID	1
		15:12	MAJOR_REV	3
		11:8	BRANCH_REV	0
		7:0	MINOR_REV	7
0x10	DIM_CA_PAD_CFG0	31:0	–	0x20222240
		31	CA_DDR_MODE1	0
		30	CA_DDR_MODE0	0
		29	CA_LV_MODE	1
		28	CA_ODT_ENA	0
		27:26	CA_ODT	0
		25:24	CA_PULL	0
		23:22	Reserved	0
		21:20	CA_NSLEW	2
		19:18	Reserved	0
		17:16	CA_PSLEW	2
		15:14	Reserved	0
		13:12	CA_NRXDEL	2
		11:10	Reserved	0
		9:8	CA_PRXDEL	2

Offset	Register name	Bits	Field name	Value
		7	CA_VM_SHIFT_ENA	0
		6:4	CA_ROUT	4
		3	Reserved	0
		2:0	CA_DCC	0
0x14	DIM_CA_PAD_CFG1	31:0	–	0x20220450
		31	CK_DDR_MODE1	0
		30	CK_DDR_MODE0	0
		29	CK_LV_MODE	1
		28	CK_CMFB_ENA	0
		27	CK_ODT_ENA1	0
		26	CK_ODT_ENA	0
		25:24	CK_ODT	0
		23:22	Reserved	0
		21:20	CK_NSLEW	2
		19:18	Reserved	0
		17:16	CK_PSLEW	2
		15:14	Reserved	0
		13	CK_CUR_MODE1	0
		12	CK_CUR_MODE0	0
		11	Reserved	0
		10:8	CK_I_DRV	4
		7	CK_VM_SHIFT_ENA	0
		6:4	CK_ROUT	5
		3	Reserved	0
		2:0	CK_DCC	0

Offset	Register name	Bits	Field name	Value
0x18	DIM_CA_PAD_CFG2	31:0	–	0x10000000
		31:30	Reserved	0
		29	VREF_LDO_ENA	0
		28	VREF_PASSGATE_ENA	1
		27:24	VREF_SP_OUT	0
		23:22	Reserved	0
		21:18	VREF_SP_IN	0
		17	VREF_BYPASS_ENA	0
		16	VREF_RDIV_ENA	0
		15:14	Reserved	0
		13:8	VREF_PULLDN_SPEED_CNTL	0
		7:6	Reserved	0
		5:0	VREF_LEVEL_CNT	0
0x1C	DIM_CA_PAD_CFG3	31:0	–	0x313003FF
		31:30	CS_N_IE	0
		29:28	CS_N_OE	3
		27:26	Reserved	0
		25	CK_IE	0
		24	CK_OE	1
		23:22	CKE_IE	0
		21:20	CKE_OE	3
		19:10	CA_IE	0
		9:0	CA_OE	1023
0x20	DIM_CA_PAD_CFG4	31:0	–	0xF0F023FF
		31:30	CS_N_OE_DYN_ENA	0
		29:28	CS_N_OE_DYN	3
		27:24	Reserved	0

Offset	Register name	Bits	Field name	Value
		23:22	CKE_OE_DYN_ENA	0
		21:20	CKE_OE_DYN	3
		19:10	CA_OE_DYN_ENA	8
		9:0	CA_OE_DYN	1023
0x0	DIM_DQ_TOP_CFG	31:0	–	0x00000031
		31:27	Reserved	0
		26	CDC_LDO_EN	0
		25	CDC_SWITCH_RC_EN	0
		24	CDC_SWITCH_BYPASS_OFF	0
		23:21	Reserved	0
		20	IOCAL_CTRL_SEL	0
		19:17	Reserved	0
		16	RCW_EN	0
		15:14	Reserved	0
		13	DEBUG_BUS_SEL	0
		12	DEBUG_BUS_EN	0
		11:9	Reserved	0
		8	CDC_TEST_EN	0
		7:6	Reserved	0
		5	WR_PIPE_EXTEND1	1
		4	WR_PIPE_EXTEND0	1
		3:1	Reserved	0
		0	WR_CLK_SEL	1
0x4	DIM_DQ_HW_INFO	31:0	–	0x00013007
		31:20	Reserved	0
		19:16	CORE_ID	1
		15:12	MAJOR_REV	3

Offset	Register name	Bits	Field name	Value
		11:8	BRANCH_REV	0
		7:0	MINOR_REV	7
0x10	DIM_DQ_PAD_CFG0	31:0	–	0xA0222250
		31	DQ_DDR_MODE1	1
		30	DQ_DDR_MODE0	0
		29	DQ_LV_MODE	1
		28	DQ_ODT_ENA	0
		27:26	DQ_ODT	0
		25:24	DQ_PULL_B	0
		23:22	Reserved	0
		21:20	DQ_NSLEW	2
		19:18	Reserved	0
		17:16	DQ_PSLEW	2
		15:14	Reserved	0
		13:12	DQ_NRXDEL	2
		11:10	Reserved	0
		9:8	DQ_PRXDEL	2
		7	DQ_VM_SHIFT_ENA	0
		6:4	DQ_ROUT	5
		3	Reserved	0
		2:0	DQ_DCC	0
0x14	DIM_DQ_PAD_CFG1	31:0	–	0xA0222250
		31	DQ_DDR_MODE1	1
		30	DQ_DDR_MODE0	0
		29	DQ_LV_MODE	1
		28	DQ_ODT_ENA	0
		27:26	DQ_ODT	0

Offset	Register name	Bits	Field name	Value
		25:24	DQ_PULL	0
		23:22	Reserved	0
		21:20	DQ_NSLEW	2
		19:18	Reserved	0
		17:16	DQ_PSLEW	2
		15:14	Reserved	0
		13:12	DQ_NRXDEL	2
		11:10	Reserved	0
		9:8	DQ_PRXDEL	2
		7	DQ_VM_SHIFT_ENA	0
		6:4	DQ_ROUT	5
		3	Reserved	0
		2:0	DQ_DCC	0
0x18	DIM_DQ_PAD_CFG2	31:0	–	0x10000000
		31:30	Reserved	0
		29	VREF_LDO_ENA	0
		28	VREF_PASSGATE_ENA	1
		27:24	VREF_SP_OUT	0
		23:22	Reserved	0
		21:18	VREF_SP_IN	0
		17	VREF_BYPASS_ENA	0
		16	VREF_RDIV_ENA	0
		15:14	Reserved	0
		13:8	VREF_PULLDN_SPEED_CNTL	0
		7:6	Reserved	0
		5:0	VREF_LEVEL_CNT	0

Offset	Register name	Bits	Field name	Value
0x20	DIM_DQ_PAD_CFG3	31:0	–	0x10AAFF31
		31:29	Reserved	0
		28	DQS_DIFF_MODE	1
		27	RCW_ODT_ENA1	0
		26	RCW_ODT_ENA0	0
		25:24	RCW_ODT	0
		23	DQ_ODT_ENA1	1
		22	DQ_ODT_ENA0	0
		21:20	DQ_ODT	2
		19	DQS_ODT_ENA1	1
		18	DQS_ODT_ENA0	0
		17:16	DQS_ODT	2
		15:8	DQ_IE_OE	255
		7:6	Reserved	0
		5	RCW_IE_OE	1
		4	DQS_IE_OE	1
		3:2	Reserved	0
		1	DM_IE	0
		0	DM_OE	1
0x24	DIM_DQ_PAD_CFG4	31:0	–	0xA0222250
		31	RCW_DDR_MODE1	1
		30	RCW_DDR_MODE0	0
		29	RCW_LV_MODE	1
		28:26	Reserved	0
		25:24	RCW_PULL_B	0
		23:22	Reserved	0
		21:20	RCW_NSLEW	2

Offset	Register name	Bits	Field name	Value
		19:18	Reserved	0
		17:16	RCW_PSLEW	2
		15:14	Reserved	0
		13:12	RCW_NRXDEL	2
		11:10	Reserved	0
		9:8	RCW_PRXDEL	2
		7	RCW_VM_SHIFT_ENA	0
		6:4	RCW_ROUT	5
		3	Reserved	0
		2:0	RCW_DCC	0
0x034	DIM_CA_CDC_CTLR_CFG1	31:0	–	0x3011111
		26:24	OSC_COUNT_DELAY	3
		22:20	STANDBY_DELAY	0
		18:16	DEL_MODE_DELAY	1
		14:12	OSC_MODE_DELAY	1
		10:8	DECODER_DELAY	1
		6:4	DIVIDER_DELAY	1
		2:0	MULTIPLIER_DELAY	1
0x038	DIM_CA_CDC_CAL_TIMER_CFG0	31:0	–	0x01201000
		24	INVALID_TIMER_ENA	1
		23:20	INVALID_TIMER_VAL	2
		16	TIMER_ENA	0
		15:0	TIMER_VAL	1000
0x03C	DIM_CA_CDC_CAL_TIMER_CFG1	31:0	–	0x00000006
		12	FF_TIMER_ENA	0
		9:0	FF_TIMER_VAL	6

Offset	Register name	Bits	Field name	Value
0x040	DIM_CA_CDC_REFCOUNT_CFG	31:0	–	0x90AD2020
		31:16	TREF	90AD
		13:8	CCAL_REF_COUNT	20
		5:0	FCAL_REF_COUNT	20
0x04C	DIM_CA_CDC_OFFSET_CFG	31:0	–	0x00000000
		20	SUBUNIT_OFFSET_MODE	0
		19	SUBUNIT_OFFSET_SIGN	0
		16:12	SUBUNIT_OFFSET	0
		8	UNIT_OFFSET_MODE	0
		7	UNIT_OFFSET_SIGN	0
		5:0	UNIT_OFFSET	0
0x050	DIM_CA_CDC_DELAY_CFG	31:0	–	0x000001D5
		28	TARGET_COUNT_ENA	0
		27:16	TARGET_COUNT	0
		11:0	DELAY_VAL	1D5
0x054	DIM_CA_CDC_SW_MODE_CFG	31:0	–	0x0
		3	SW_DEL_MODE	0
		2	SW_OSC_MODE	0
		1	SW_DA_SEL	0
		0	SW_LOAD	0
0x05C	DIM_CA_CDC_SW_OVRD_CFG	31:0	–	0x00000000
		16	SW_REF_GATE	0
		11	SW_OVRD_DA1_OSC_EN	0
		10	SW_OVRD_DA1_IN_EN	0
		9	SW_OVRD_DA0_OSC_EN	0
		8	SW_OVRD_DA0_IN_EN	0
		3	SW_OVRD_CDC_COUNTER_RST	0

Offset	Register name	Bits	Field name	Value
		2	SW_OVRD_LOAD_DA_SEL	0
		1	SW_OVRD_ACTV_DA_SEL	0
		0	SW_OVRD_ENA	0
0x034	DIM_DQ_CDC_CTLR_CFG1	31:0	–	0x3011111
		26:24	OSC_COUNT_DELAY	3
		22:20	STANDBY_DELAY	0
		18:16	DEL_MODE_DELAY	1
		14:12	OSC_MODE_DELAY	1
		10:8	DECODER_DELAY	1
		6:4	DIVIDER_DELAY	1
		2:0	MULTIPLIER_DELAY	1
0x038	DIM_DQ_CDC_CAL_TIMER_CFG0	31:0	–	0x01201000
		24	INVALID_TIMER_ENA	1
		23:20	INVALID_TIMER_VAL	2
		16	TIMER_ENA	0
		15:0	TIMER_VAL	1000
0x03C	DIM_DQ_CDC_CAL_TIMER_CFG1	31:0	–	0x00000006
		12	FF_TIMER_ENA	0
		9:0	FF_TIMER_VAL	6
0x040	DIM_DQ_CDC_REFCOUNT_CFG	31:0	–	0x90AD2020
		31:16	TREF	90AD
		13:8	CCAL_REF_COUNT	20
		5:0	FCAL_REF_COUNT	20
0x04C	DIM_DQ_RD_CDC_OFFSET_CFG	31:0	–	0x00000000
		20	SUBUNIT_OFFSET_MODE	0
		19	SUBUNIT_OFFSET_SIGN	0
		16:12	SUBUNIT_OFFSET	0

Offset	Register name	Bits	Field name	Value
		8	UNIT_OFFSET_MODE	0
		7	UNIT_OFFSET_SIGN	0
		5:0	UNIT_OFFSET	0
0x050	DIM_DQ_RD_CDC_DELAY_CFG	31:0	–	0x000001D5
		28	TARGET_COUNT_ENA	0
		27:16	TARGET_COUNT	0
		11:0	DELAY_VAL	1D5
0x054	DIM_DQ_RD_CDC_SW_MODE_CFG	31:0	–	0x00000000
		3	SW_DEL_MODE	0
		2	SW_OSC_MODE	0
		1	SW_DA_SEL	0
		0	SW_LOAD	0
0x05C	DIM_DQ_RD_CDC_SW_OVRD_CFG	31:0	–	0x00000000
		16	SW_REF_GATE	0
		11	SW_OVRD_DA1_OSC_EN	0
		10	SW_OVRD_DA1_IN_EN	0
		9	SW_OVRD_DA0_OSC_EN	0
		8	SW_OVRD_DA0_IN_EN	0
		3	SW_OVRD_CDC_COUNTER_RST	0
		2	SW_OVRD_LOAD_DA_SEL	0
		1	SW_OVRD_ACTV_DA_SEL	0
		0	SW_OVRD_ENA	0
0x060	DIM_DQ_RD_CDC_SLAVE_DDA_CFG	31:0	–	0x0001626C
		17	SLAV_DDA_OFFSET_MODE	0
		16	SLAV_DDA_OFFSET_SIGN	1
		15:12	SLAVE_DDA_OFFSET	6
		10:0	SLAVE_DDA_DELAY	26C

Offset	Register name	Bits	Field name	Value
0x0AC	DIM_DQ_WR_CDC_OFFSET_CFG	31:0	–	0x00000000
		20	SUBUNIT_OFFSET_MODE	0
		19	SUBUNIT_OFFSET_SIGN	0
		16:12	SUBUNIT_OFFSET	0
		8	UNIT_OFFSET_MODE	0
		7	UNIT_OFFSET_SIGN	0
		5:0	UNIT_OFFSET	0
0x0B0	DIM_DQ_WR_CDC_DELAY_CFG	31	–	0x000001D5
		28	TARGET_COUNT_ENA	0
		27:16	TARGET_COUNT	0
		11:0	DELAY_VAL	1D5
0x0B4	DIM_DQ_WR_CDC_SW_MODE_CFG	31	–	0x00000000
		3	SW_DEL_MODE	0
		2	SW_OSC_MODE	0
		1	SW_DA_SEL	0
		0	SW_LOAD	0
0x0BC	DIM_DQ_WR_CDC_SW_OVRD_CFG	31	–	0x00000000
		16	SW_REF_GATE	0
		11	SW_OVRD_DA1_OSC_EN	0
		10	SW_OVRD_DA1_IN_EN	0
		9	SW_OVRD_DA0_OSC_EN	0
		8	SW_OVRD_DA0_IN_EN	0
		3	SW_OVRD_CDC_COUNTER_RST	0
		2	SW_OVRD_LOAD_DA_SEL	0
		1	SW_OVRD_ACTV_DA_SEL	0
		0	SW_OVRD_ENA	0

2.2.4 Recommended settings for clock frequency-dependent APQ8064E registers

Certain register settings depend on the APQ8064E clock frequency. This section lists these clock frequency-dependent registers. Table 2-6 lists these register settings for the EBI bus clock frequency of 533 MHz.

Table 2-6 Clock frequency-dependent register settings for EBI0/EBI1 at 533 MHz

Offset	Register name	Bits	Field name	Value
0x80058	DDR_DRAM_TIMING_0	31:0	–	0x5B706634
		31:29	TRTP	2
		28:24	TFAW	27
		23:20	TRCD	7
		19:16	Reserved	0
		15:12	TRRD	6
		11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	3
		8:7	Reserved	0
		6:5	tZQCL_MSB	1
		4:0	TRAS_MIN	20
0x8005C	DDR_DRAM_TIMING_1	31:0	–	0x00044044
		31:30	Reserved	0
		29	INCL_DARF_MAX_NUM_ACT_RANK1	0
		28	INCL_DARF_MAX_NUM_ACT_RANK0	0
		27:20	Reserved	0
		19:16	MAX_NUM_ACT_RANK1	4
		15:12	MAX_NUM_ACT_RANK0	4
		11:8	MAX_NUM_REFRESHES_TREFBW	0
		7	Reserved	0
		6:4	TMRD_READS	4
		3	Reserved	0
		2:0	TMRD_WRITES	4

Offset	Register name	Bits	Field name	Value
0x80060	DDR_DRAM_TIMING_2	31:0	–	0xEA0C3222
		31:21	TRAS_MAX	1872
		20:18	TCKE	3
		17:15	Reserved	0
		14:12	WR_TO_RD_DLY_DIFF_RANK	3
		11	Reserved	0
		10:8	TRTW_SAME_RANK	2
		7	Reserved	0
		6:4	TRTW_DIFF_RANK	2
		3	Reserved	0
		2:0	TOST	2
0x80064	DDR_DRAM_TIMING_3	31:0	–	0xD4440040
		31:28	PD_EXIT_DURATION_ODT	13
		27:24	TWTR	4
		23	Reserved	0
		22:19	TWR	8
		18:9	TXSRD	512
		8	Reserved	0
		7:0	TXSNR	64
0x80068	DDR_DRAM_TIMING_4	31:0	–	0x3BC44D40
		31:24	TRFC	59
		23:20	TMOD	12
		19:16	TXPNR_ACT_PWR_DOWN	4
		15:12	TXPR_ACT_PWR_DOWN	4
		11:8	TXPNR_PCHG_PWR_DOWN	13
		7:4	TXPR_PCHG_PWR_DOWN	4
		3:2	Reserved	0

Offset	Register name	Bits	Field name	Value
		1	TXPNR_PCHG_PWR_DOWN_MSB	0
		0	TXPR_PCHG_PWR_DOWN_MSB	0
0x8006C	DDR_DRAM_TIMING_5	31:0	–	0x03667077
		31:24	SELF_RFSH_MIN_DURATION	3
		23	Reserved	0
		22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	6
		19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	6
		15:12	TRP_AB	7
		11:8	Reserved	0
		7:4	TRP_PB	7
		3:0	RD_LATENCY	7
0x80070	DDR_DRAM_TIMING_6	31:0	–	0x60212000
		31:28	WR_LATENCY	6
		27:24	Reserved	0
		23:20	RESTART_CLK_PWR_DOWN_EXIT	2
		19	Reserved	0
		18:16	STOP_CLK_PWR_DOWN_ENTRY	1
		15:14	Reserved	0
		13:12	TSRR	2
		11:8	Reserved	0
		7:4	Reserved	0
		3:0	Reserved	0
0x80074	DDR_DRAM_TIMING_7	31:0	–	0x00811F64
		31:24	TZQCL	0
		23:17	TZQCS	48
		16	PAD_LOW_POWER_MODE	1
		15:12	DLY_RD_CAPTURE	1

Offset	Register name	Bits	Field name	Value
		11:8	EXT_RD_CAPTURE	15
		7:4	DLY_IE_START	6
		3:0	EXT_IE_WINDOW	4
0x80078	DDR_DRAM_TIMING_8	31:0	–	0x01010101
		31:30	Reserved	0
		29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	0
		27:24	RCW_START_DLY_BYTE3	1
		23:22	Reserved	0
		21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	0
		19:16	RCW_START_DLY_BYTE2	1
		15:14	Reserved	0
		13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	0
		11:8	RCW_START_DLY_BYTE1	1
		7:6	Reserved	0
		5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	0
		3:0	RCW_START_DLY_BYTE0	1
0x8007C	DDR_DRAM_TIMING_9	31:0	–	0x00000000
		31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	0
		23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	0
		15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	0
		7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	0
0x80080	DDR_DRAM_TIMING_0_ALT	31:0	–	0x5B70634
		31:29	TRTP	2
		28:24	TFAW	27
		23:20	TRCD	7
		19:16	Reserved	0
		15:12	TRRD	6

Offset	Register name	Bits	Field name	Value
		11:9	PWR_DOWN_ODT_OFF_MAX_MIN_DIFF	4
		8:7	Reserved	0
		6:5	tZQCL_MSB	1
		4:0	TRAS_MIN	20
0x80084	DDR_DRAM_TIMING_3_ALT	31:0	–	0xD4440040
		31:28	PD_EXIT_DURATION_ODT	13
		27:24	TWTR	4
		23	Reserved	0
		22:19	TWR	8
		18:9	TXSRD	512
		8	Reserved	0
		7:0	TXSNR	64
0x80088	DDR_DRAM_TIMING_4_ALT	31:0	–	0x3BC44D40
		31:24	TRFC	59
		23:20	TMOD	12
		19:16	TXPNR_ACT_PWR_DOWN	4
		15:12	TXPR_ACT_PWR_DOWN	4
		11:8	TXPNR_PCHG_PWR_DOWN	13
		7:4	TXPR_PCHG_PWR_DOWN	4
		3:2	Reserved	0
		1	TXPNR_PCHG_PWR_DOWN_MSB	0
		0	TXPR_PCHG_PWR_DOWN_MSB	0
0x8008C	DDR_DRAM_TIMING_5_ALT	31:0	–	0x03667077
		31:24	SELF_RFSH_MIN_DURATION	3
		23	Reserved	0
		22:20	CLK_STOP_AFTER_SELF_RFSH_ENTRY	6
		19:16	CLK_RESTART_BEFORE_SELF_RFSH_EXIT	6

Offset	Register name	Bits	Field name	Value
		15:12	TRP_AB	7
		11:8	Reserved	0
		7:4	TRP_PB	7
		3:0	RD_LATENCY	7
0x80090	DDR_DRAM_TIMING_7_ALT	31:0	–	0x00811F64
		31:24	TZQCL	0
		23:17	TZQCS	64
		16	PAD_LOW_POWER_MODE	1
		15:12	DLY_RD_CAPTURE	1
		11:8	EXT_RD_CAPTURE	15
		7:4	DLY_IE_START	6
		3:0	EXT_IE_WINDOW	4
0x80094	DDR_DRAM_TIMING_8_ALT	31:0	–	0x01010101
		31:30	Reserved	0
		29:28	RCW_CFG_COARSE_DLY_DATA_BYTE3	0
		27:24	RCW_START_DLY_BYTE3	1
		23:22	Reserved	0
		21:20	RCW_CFG_COARSE_DLY_DATA_BYTE2	0
		19:16	RCW_START_DLY_BYTE2	1
		15:14	Reserved	0
		13:12	RCW_CFG_COARSE_DLY_DATA_BYTE1	0
		11:8	RCW_START_DLY_BYTE1	1
		7:6	Reserved	0
		5:4	RCW_CFG_COARSE_DLY_DATA_BYTE0	0
		3:0	RCW_START_DLY_BYTE0	1

Offset	Register name	Bits	Field name	Value
0x80098	DDR_DRAM_TIMING_9_ALT	31:0	–	0x00000000
		31:24	RCW_CFG_FINE_DLY_DATA_BYTE3	0
		23:16	RCW_CFG_FINE_DLY_DATA_BYTE2	0
		15:8	RCW_CFG_FINE_DLY_DATA_BYTE1	0
		7:0	RCW_CFG_FINE_DLY_DATA_BYTE0	0
0x8009C	DDR_UPDATE_FREQ_CHANGE_ALT	31:0	–	0x600B800A
		31:28	WR_LATENCY	6
		27:22	Reserved	0
		21:19	ODT_START_DELAY_WR	1
		18:16	ODT_START_DELAY_RD	3
		15:13	ODT_OFF_DELAY	4
		12:4	Reserved	0
		3:1	tANPD	5
		0	Reserved	0

EXHIBIT 1

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