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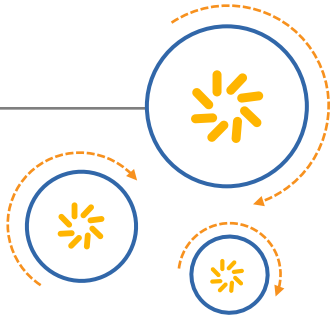

AR6004 Single Chip 2X2 802.11 A/B/G/N MIMO MAC/BB/Radio

Data Sheet

September 2016

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Revision history

Revision	Date	Description
B	September 2016	Change title by removing: Qualcomm Snapdragon 600 (APQ8064) Section 1.1: changed the term ‘mobile applications’ to ‘embedding computing’ Section 1.1: Added two notes Table A-1: Added acronyms and definitions
A	June 1, 2015	Initial Release

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1 Introduction

1.1 General description

The AR6004 is a single chip, small form factor 2x2 IEEE 802.11 a/b/g/n MAC/baseband/radio optimized for low-power embedded computing. It is the fourth generation WLAN design in the ROCm family, employing low power consumption WLAN architecture in the smallest possible form factor. The AR6004 is a two-stream 2x2 dual-band MIMO 802.11n implementation. The AR6004 provides improved link robustness, extended range, increased throughput, and better performance at home, at work, or while mobile. The AR6004 is part of the XSpan product family. It provides high wireless throughput, enabling flawless media stream and file sharing on any Wi-Fi device. The AR6004 family implements design techniques to deliver a solution that will extend the battery life of mobile and embedded systems. It leverages its near-zero power in idle and stand-by modes to enable users to leave WLAN *always-on* without impacting battery life.

The AR6004 family offers silicon integration and implements proprietary internal efficient power amplifier (EPA) technology in CMOS with advanced linearization algorithms and internal low-noise amplifiers (LNAs), thereby reducing the BOM costs in the system design. It provides the option for an additional external PA for higher output power if needed. The AR6004 family has an integrated power management unit (PMU) that allows the AR6004 to be powered directly from the battery. It has an on-chip switching regulator for voltage conversion and additional LDOs to provide noise isolation for digital and analog supplies.

The AR6004 family supports 2- and 3-wire and proprietary BT coexistence protocols with advanced algorithms for predicting channel usage by a colocated BT transceiver.

The AR6004 family provides multiple peripheral interfaces (PIFs) including universal asynchronous receiver/transmitter (UART), SDIO, SPI, I2C, etc., using GPIO pins. The only external clock source needed for AR6004-based designs is a high-speed crystal or oscillator. A variety of reference clocks are supported that include 19.2, 24, 26, 38.4, 40 and 52 MHz. AR6004 chips are available in wafer-level chip scale packages (WLCSP) or 6x6 ball grid arrays (BGA) packaging.

NOTE: This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE: Enabling some features may require additional licensing fees.

1.2 AR6004 features

- All-CMOS IEEE 802.11a/b/g/n or 802.11b/ g/n single-chip client
- Two-stream 802.11n to provide highest throughput and superior radio frequency (RF) performance for devices
- Advanced 2x2 802.11n features:
  - 40 MHz channels at 5GHz
  - Full/Half guard interval
  - Frame aggregation
  - Space time block coding (STBC)
  - Low density parity check (LDPC)
  - Maximum ratio combining (MRC)
  - Transmit beamforming (TxBF)
  - Maximum likelihood (ML) decoder
- Integrated high-output EPA and LNA for lowest BOM
- Support of popular interfaces used in embedded designs: SDIO v2.0 (50 MHz, 4-bit and 1-bit), USB, HSIC and GSPI
- Low-power consumption with near zero in idle/standby modes, extending battery life
- Support of indoor location when paired with GPS
- Integrated on-chip processor to minimize the loading on host processor
- Support of 2/3-wire enhanced packet traffic arbitration (PTA) scheme Bluetooth (BT) solution for optimal coexistence implementation
- PTA scheme and BT coexistence protocol with BT solution
- Support of multiple reference clocks from 19.2 MHz to 52 MHz
- Optional external PA, LNA
- Data rates of up to 54 Mb/s for 802.11a/g and 144.4 Mb/s for 802.11n HT20, 300 Mb/s for HT40
- Advanced power management to minimize standby, sleep and active power
- Security support for WPS, WPA2, WPA, WAP and protected management frames
- Full 802.11e QoS support including Wi-Fi Multimedia (WMM) and U-APSD
- Low-power listen mode for reduced receive power consumption and sleep current
- Green-Tx power saving
- 802.11e-compatible bursting
- Support for the IEEE 802.11e, h, i, and j

- Wired equivalent privacy (WEP), temporal key integrity protocol (TKIP), WLAN authentication and privacy infrastructure (WAPI), and advanced encryption standard (AES) hardware encryption
- Reduced (half) guard interval
- Frame aggregation with A-MPDU
- Support of round-trip time (RTT) based ranging measurement to any Wi-Fi devices, which can be used as part of hybrid location system (HLS) for indoor positioning

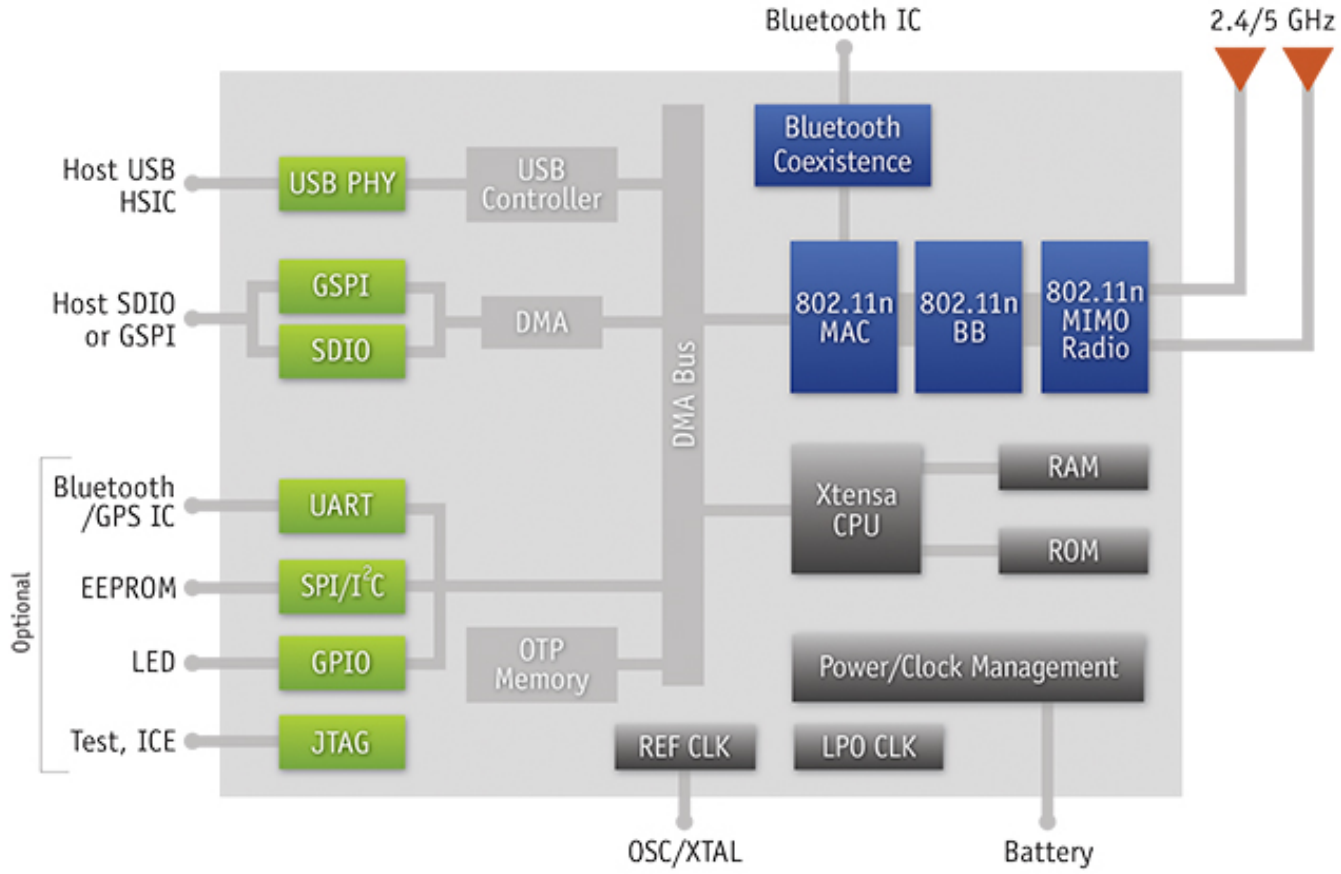

Figure 1-1 AR6004 system block diagram

2 Functional Description

2.1 Overview

The AR6004 is a single chip 2x2 802.11 a/b/g/n device, optimized for low-power embedded applications with dual-stream capability for both transmit and receive. Frame aggregation, reduced inter-frame spacing (RIFS) and half-guard intervals provide improved throughput on the link. The AR6004 provides a robust communication environment, capable of supporting STBC LDPC codes. Additional 11n performance optimizations, such as 11n frame aggregation (A-MPDU and A-MSDU) are provided by drivers that support SDIO bus transaction bundling (a form of bus aggregation) and low-overhead host assisted buffering (RX A-MSDU and RX A-MPDU). These techniques can improve the performance and efficiency of applications involving large bulk data transfers (for example, file transfers or high-resolution video streaming). The typical data path consists of the host interface, mailbox DMA, advanced high-performance bus (AHB), memory controller, MAC, baseband module (BB), and radio. The CPU drives the control path using register and memory accesses. External interfaces include USB, HSIC (with LPM support), SDIO or GSPI, reference clock, and front-end components as well as optional connections such as UART, SPI/I2C, GPIO, JTAG, 32 kHz source (see Figure 1-1).

2.2 XTENSA CPU

At the heart of the chip is the XTENSA CPU. The CPU is connected to a large 288 KB RAM block, which precludes the need of an external memory. The CPU has 512 KB internal ROM. The CPU connects to the main AHB bus through its peripheral interface. It also has a JTAG interface for debugging.

The CPU's internal logic and boot code are designed to detect the presence of an external host and to automatically begin communicating with that host. The CPU communicates directly with the RAM and ROM modules within the device without any caching. Boot code in the 512 KB ROM first detects the presence of an external host. It then begins communicating with this host.

2.3 AHB and APB blocks

The AHB block acts as an arbiter on the AHB bus and arbitrates requests from various components of the chip. Depending upon the address, the AHB data request can go into one of the two slaves: APB block or the CPU PIF. Data requests to the CPU PIF are generally high-speed memory requests, while requests to the APB block are primarily meant for register access.

The APB block acts as a decoder. It is meant only for access to programmable registers within the AR6004's main blocks. Depending on the address, the APB request can go to one of the places listed below:

- Radio
- SI/SPI
- MBOX
- GPIO
- UART
- Real time clock (RTC)
- MAC/BB

2.4 Master SI/SPI control

The AR6004 has a master serial interface (SI) that can operate in two, three, or four-wire bus configurations to control EEPROMs or other I2C/SPI devices. Multiple I2C devices with different device addresses are supported by sharing the two-wire bus. Multiple SPI devices are supported by sharing the clock and data signals and using separate software-controlled GPIO pins as chip selects.

An SI transaction consists of two phases: a data transmit phase of 0-8 bytes followed by a data receive phase of 0-8 bytes. The flexible SI programming interface allows software to support various address and command configurations in I2C/SPI devices. In addition, software may operate the SI in either polling or interrupt mode.

2.5 GPIO

The AR6004 has GPIO pins with direct software access. Many pins are multiplexed with other functions, such as the host interface, UART, SI, BT coexistence, etc. (see Chapter 6 for details). Each GPIO supports the following configurations through software programming:

- Internal pull-up/down options
- Input available for sampling by a software register
- Input triggering an edge or level CPU interrupt
- Input triggering a level chip wakeup interrupt
- Open-drain or push-pull output driver
- Output source from a software register or the sigma delta pulse-width modulation (PWM) digital to analog converter (DAC)

The AR6004 has one Sigma Delta PWM DAC that is shared by all of the GPIO pins. It allows the GPIO pins to approximate intermediate output voltage levels. The DAC has a period of 256 samples with a software controllable duty cycle. In applications where the AR6004 is driving LEDs using GPIO pins, the Sigma Delta PWM DAC can provide a continuous dimmer function.

2.6 MBOX

The MBOX is a service module to handle one of two possible external hosts: SDIO or GSPI. The AR6004 can handle only one of these hosts at any given time. The type of host the AR6004 uses depends upon the polarity of some package pins upon system power-up. The MBOX has two interfaces: an APB interface for access to the MBOX registers and an AHB interface, which is used by the external host to access the MC memory or other registers within the AR6004.

2.7 HCI UART over SDIO – BT and GPS

The AR6004 has a high-speed UART that is intended to connect to an external BT chip through its HCI interface. This UART can directly transfer data between the host and BT or GPS device.

2.8 Debug UART

The AR6004 includes a high-speed UART interface that is fully compatible with the 16550 UART industry standard. This UART is a general purpose UART although it is primarily used for debug.

2.9 Reset control

The AR6004 CHIP_PWD_L pin can be used to completely reset the entire chip. After this signal has been de-asserted, the AR6004 waits for host communication. Until then, the MAC, BB, and SOC blocks are powered off and all modules except the host interface are held in reset.

Once the host has initiated communication, the AR6004 turns on its crystal and later on its PLL. After all clocks are stable and running, the resets to all blocks are automatically de-asserted.

2.10 Reset sequence

After a COLD_RESET event (for example, the host toggles CHIP_PWD_L) the AR6004 enters the HOST_OFF state and awaits communication from the host. From that point, the typical AR6004 COLD_RESET sequence is listed below:

1. When the host is ready to use the AR6004, it initiates communication through SDIO or GSPI.
2. The AR6004 enters the WAKEUP state then the ON state and enables the XTENSA CPU to begin executing ROM code. Software configures the AR6004 functions and interfaces. When the AR6004 is ready to receive commands from the host, it sets an internal function ready bit.
3. The host reads the ready bit and can send function commands to the AR6004.
4. The CPU may continue to be held in reset under some circumstances until its reset is cleared by an external pin or when the host clears a register.
5. The MAC cold reset and the MAC/BB warm reset continues to stay asserted until their respective reset registers are cleared by software.

2.11 Power management unit

The AR6004 has an integrated PMU that generates all the power supplies required by its internal circuitry, either from an external battery or a 3.3 V supply.

The main components of the PMU include the following:

- A linear regulator (PAREG) that converts the battery power to a 3.3 V supply, which can be bypassed if a 3.3 V supply is already available.
- A switching regulator (SWREG) that produces a 1.2 V supply from the 3.3 V supply.
- A linear regulator (SREG) that converts the host I/O supply to a 1.2 V supply for some small control blocks, which are turned on when CHIP_PWD_L is de-asserted.

2.12 Power transition diagram

The AR6004 provides integrated power management and control functions and extremely low-power operation for maximum battery life across all operational states by:

- Gating clocks for logic when not needed
- Shutting down unneeded high-speed clock sources
- Reducing voltage levels to specific blocks in some states

2.12.1 Hardware power states

AR6004 hardware has five top-level hardware power states managed by the RTC block. Table 2-1 describes the input from the MAC, CPU, SDIO/MBOX, interrupt logic, and timers that affect the power states.

2.12.2 Sleep state management

Sleep state minimizes power consumption while saving system states. In SLEEP state, all high speed clocks are gated off and the external reference clock source is powered off. For the AR6004 to enter SLEEP state, the MAC, MBOX, and CPU systems must not be active.

The system remains in sleep state until a WAKEUP event causes the system to enter WAKEUP state, wait for the reference clock source to stabilize, and then ungate all enabled clock trees. The CPU wakes up only when an interrupt arrives, which may have also generated the system WAKEUP event.

Table 2-1 Power management states

State	Description
OFF	CHIP_PWD_L pin assertion immediately brings the chip to this state.
	Sleep clock is disabled.
	No state is preserved.

State	Description
HOST_OFF	WLAN is off. Only the SDIO host interface is powered on, the rest of the chip is power gated (off).
	Sharing the WLAN's reference clock with a collocated device is supported, provided the AVDD33 supply is available. Clock sharing will increase consumption in this mode by 2 mA at 3.3 V.
	The host can transition AR6004 to WAKEUP (followed by ON) at any time by writing a register in the host interface domain.
	WLAN and CPU state are not retained.
	For USB/HSIC or hostless designs, this state is bypassed by pulling GPIO0 low at the deassertion of CHIP_PWD_L. This state applies only to SDIO designs.
SLEEP	Only the sleep clock is operating.
	The crystal or oscillator is disabled.
	Any wakeup events (MAC, host, LF timer, GPIO interrupt force a transition to WAKEUP.
	All internal states are maintained.
	Host interface is idle (USB is in SUSPEND).
WAKEUP	The system transition from sleep OFF states to ON.
	The high frequency clock is gated off as the oscillator is brought up and the PLL is enabled.
	WAKEUP duration is usually 2 ms.
ON	The high speed clock is operational and sent to each block enabled by the clock control register.
	Lower-level clock gating is implemented at the block level, including the CPU, which can be gated off using WAITI instructions while the system is on. No CPU, host or WLAN activities go to sleep.

Figure 2-1 shows the power state transition diagram.

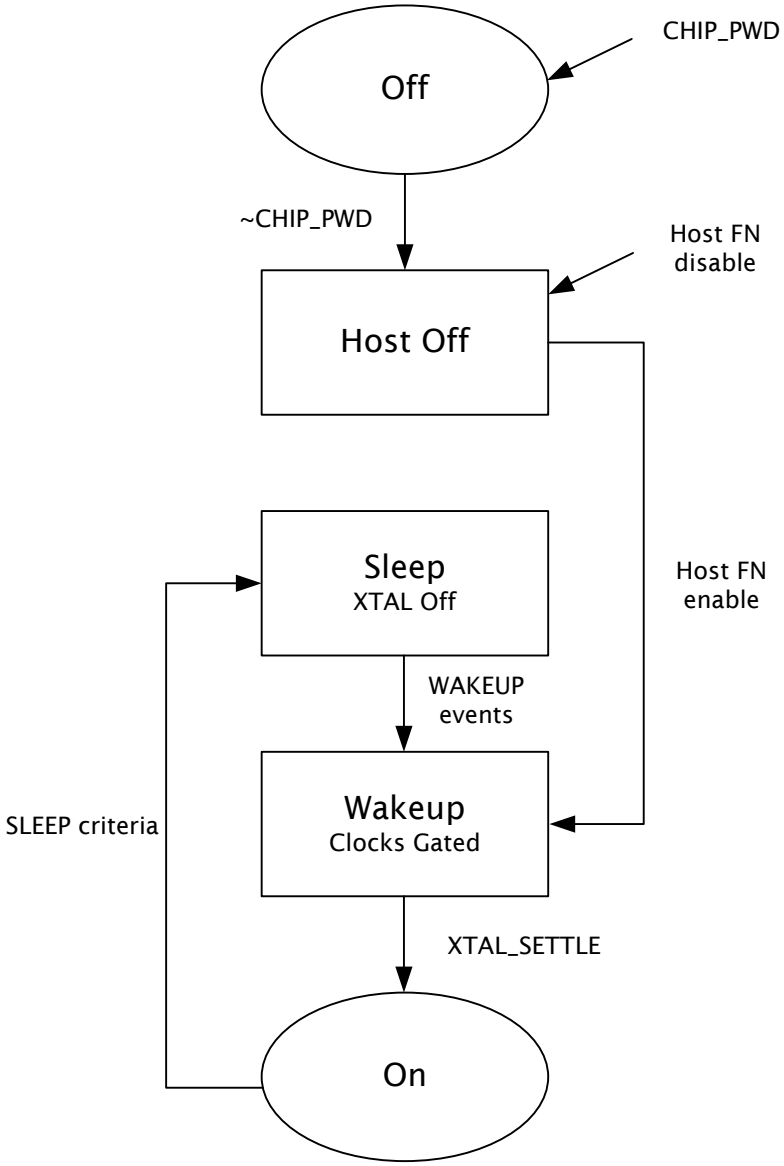

Figure 2-1 AR6004 power state

2.13 System clocking (RTC block)

The AR6004 has an RTC block that controls the clocks and power going to other internal modules. Its inputs consist of sleep requests from these modules and its outputs consists of clock enable and power signals, which are used to gate the clocks going to these modules. The RTC block also manages resets going to other modules with the device. The AR6004's clocking is grouped into two types:

- High-speed
- Low-speed

2.13.1 High-speed clocking

The reference clock source drives the PLL and RF synthesizer within the AR6004. It can be either an external crystal or oscillator. To minimize power consumption, the reference clock source is powered off in SLEEP, HOST_OFF, and OFF states. For an external crystal, the AR6004 disables the on-chip oscillator driver. For an external oscillator, the AR6004 de-asserts its CLK_REQ signal to indicate that a reference clock is not needed.

When exiting SLEEP state, the AR6004 waits in WAKEUP state for a programmable duration. During this time, the CLK_REQ signal is asserted to allow for the reference clock source to settle. The CLK_REQ signal remains asserted in ON state.

The AR6004 supports reference clock sharing in all power states. For an external crystal, the on-chip oscillator driver drives a reference clock output whenever an external clock request signal is asserted. For an external oscillator, the external clock request signal is forwarded on the CLK_REQ signal, and the input clock is passed along to the reference clock output.

2.13.2 Low-speed clocking

The AR6004 has eliminated the need for an external sleep clock source thereby reducing system cost. Instead, an internal ring oscillator is used to generate a low-frequency sleep clock. It is also used to run the state machines and counters related to low power states.

The AR6004 has an internal calibration module that produces a 32.768 KHz output with minimal variation. For this, it uses the reference clock source as the golden clock. As a result, the calibration module adjusts for process and temperature variations in the ring oscillator when the system is in ON state.

The AR6004 also supports using an external low-frequency sleep clock source in applications where one is already available.

2.13.3 Interface clock

The host interface clock represents another clock domain for the AR6004. This clock comes from the SDIO or GSPI host and is completely independent from the other internal clocks. This clock drives the host interface logic as well as certain registers that can be accessed by the host in HOST_OFF and SLEEP states.

2.14 Front-end control

For applications that use external front-end components, the AR6004 provides the ability to control them with four antenna switch control outputs named as follows:

- ANTA
- ANTB
- ANTC
- ANTD

A programmable switch table indexed by transceiver state offers flexibility for various front-end configurations. The AR6004 supports antenna sharing with another wireless chip in all power states by using ANTD to control the shared antenna switch.

2.15 MAC/BB/RF block

The AR6004 wireless MAC consists of five major blocks:

- Host interface unit (HIU) for bridging to the AHB for bulk data accesses and APB for register accesses
- Ten queue control units (QCU) for transferring Tx data
- Ten DCF control units (DCU) for managing channel access
- Protocol control unit (PCU) for interfacing to baseband
- DMA receive unit (DRU) for transferring Rx data

2.16 Baseband block

The AR6004 BB is the physical layer controller for the 802.11a/b/g/n air interface. The AR6004 BB is responsible for modulating data packets in the transmit direction, and detecting and demodulating data packets in the receive direction. It has a direct control interface to the radio to enable hardware to adjust analog gains and modes dynamically.

2.17 Design for test

The AR6004 has a built-in JTAG boundary scan of its pins. It also has features that enable testing of digital blocks using ATPG scan, memories using MBIST, analog components, and the radio.

2.18 Active power save

2.18.1 Low-power listen

To minimize active current consumption, the AR6004 firmware will set the receiver in a low-power listen (LPL) mode, thus saving active power in between frames, when the transceiver is awaiting frames, as well as during active reception. It can be enabled in most conditions with minimal performance impact, between 1 and 2 dB. If harsh channel conditions require it, firmware will automatically revert to full power mode.

2.18.2 Green Tx

To minimize active current consumption during transmission, the AR6004 utilizes Green transmitter (Tx). This feature allows the device to save power when communicating with a nearby station or access point when high-output power is not required to sustain long range. In such cases, the Tx reduces the transmit power for current saving, while maintaining its high uplink throughput.

3 Radio

The AR6004 transceiver consists of the following major functional blocks (see Figure 3-1):

- Receiver (Rx)
- Transmitter (Tx)
- Frequency synthesizer (SYNTH)
- Associated bias/control (BIAS)
- PMU

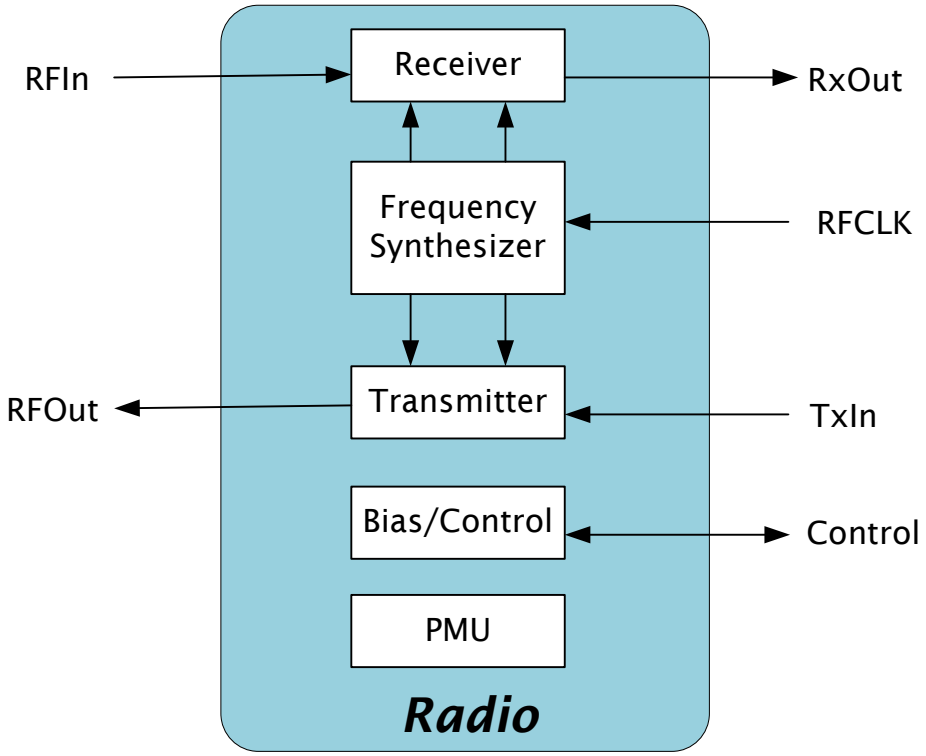

Figure 3-1 Radio functional block diagram

3.1 Receiver block

The receiver converts an RF signal (with 40 MHz maximum bandwidth) to baseband I and Q outputs. The receiver is tuned to 2.4 GHz and 5 GHz for IEEE 802.11 b/g/n and 802.11a/n signals, respectively. Figure 3-2 shows the radio Tx/Rx block diagram.

For 5 GHz operation, the receiver is comprised of a low noise amplifier (LNA) followed by a variable gain amplifier (VGA), a radio frequency (RF) mixer, an intermediate frequency (IF) mixer, and a baseband programmable gain filter. This receiver is implemented using the sliding IF topology.

For 2 GHz operation, the receiver is comprised of an LNA, a direct conversion mixer, and a baseband programmable gain filter. This receiver is implemented using the direct conversion topology.

For both 5 GHz and 2 GHz paths, mixers down convert the signal to baseband in-phase (I) and quadrature-phase (Q) signals. The I and Q signals are low-pass filtered and amplified by the baseband programmable gain filter controlled by digital logic. The baseband I and Q signals are sent to the ADC. The baseband programmable gain filter is shared between the 2 GHz and 5 GHz paths.

The DC offset of the receive chain is reduced using multiple DACs controlled by the MAC/baseband block. In addition, the receive chain can be digitally powered down to conserve power.

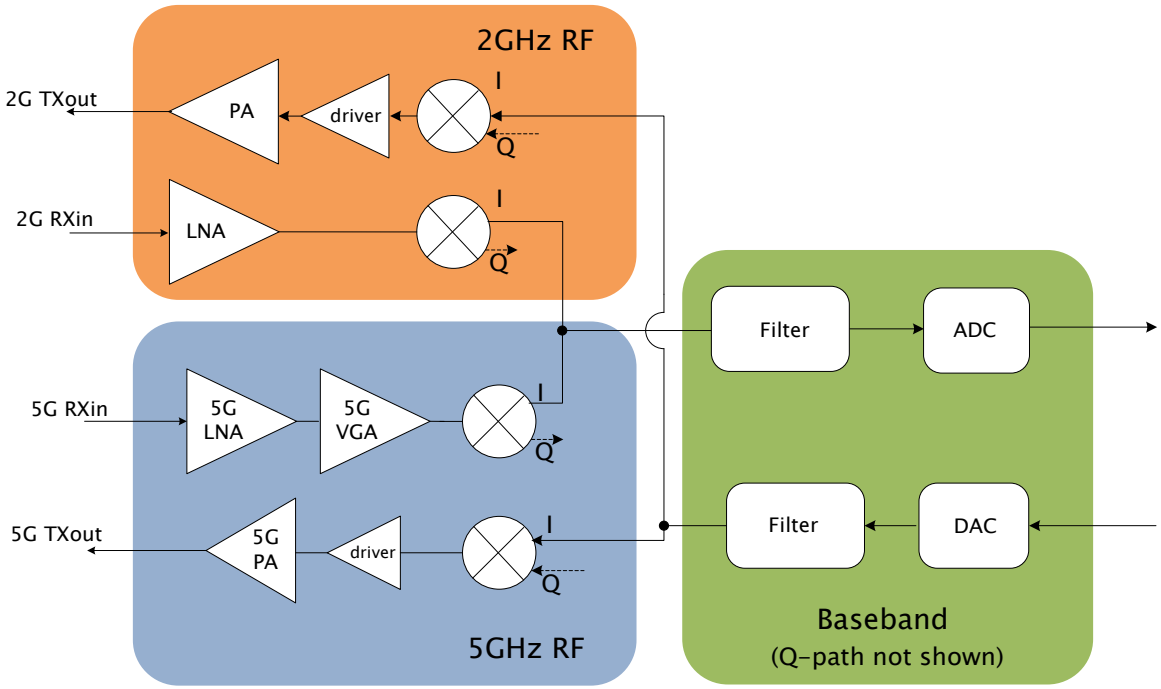

Figure 3-2 Radio Tx/Rx block diagram

3.2 Tx block

The Tx converts baseband I and Q inputs to bands centered around 2.4 GHz and 5 GHz for IEEE 802.11 b/g/n and 802.11a/n signals respectively. A block diagram is shown in Figure 3-2.

The outputs of the DAC are low pass filtered through an on-chip reconstruction filter to remove spectral images and out-of-band quantization noise.

For 5 GHz operation, the Tx is comprised of a programmable reconstruction filter, an IF mixer, an RF mixer, a preamplifier and a PA. The IF mixer converts baseband signals to an IF. The RF mixer converts the IF signal into radio frequency signals, which are driven off chip through a preamplifier and the PA. This Tx is implemented using the sliding IF topology.

For 2 GHz operation, the Tx is comprised of a programmable reconstruction filter, a direct conversion mixer, a preamplifier and a PA. This Tx is implemented using the direct conversion topology.

The transmit chain can be digitally powered down to conserve power. To ensure that FCC limits are observed and that output power stays close to the maximum allowed, the transmit output power is adjusted by a digitally programmable control loop at the start of each packet. The power control can also compensate for temperature variation.

3.3 Synthesizer (SYNTH) block

The radio supports an on-chip synthesizer to generate local oscillator (LO) frequencies for the receiver and Tx mixers. Figure 3-3 shows the synthesizer topology.

The synthesizer can use several crystals such as 19.2, 24, 26, 38.4, 40, and 52 MHz. For AR6004, the default crystal frequency is 26 MHz.

A reference circuitry generates a signal used as the synthesizer reference input. An on-chip voltage controlled oscillator (VCO) provides the desired LO signal based on a phase/frequency locked loop. The loop filter components are all integrated on-chip and can be digitally controlled.

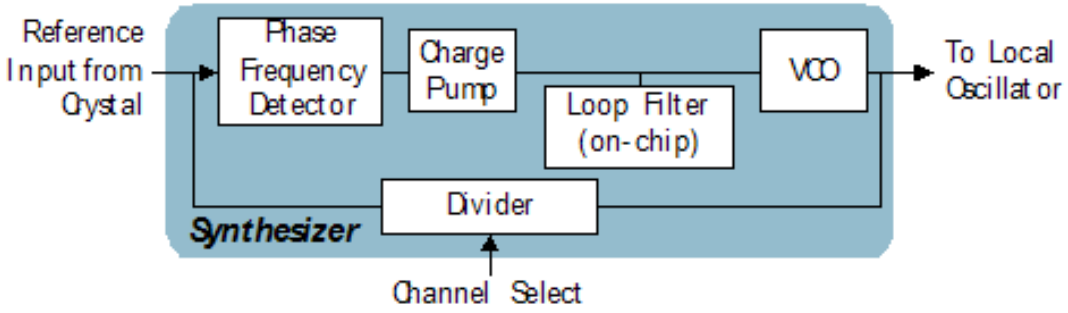

Figure 3-3 Radio synthesizer block diagram

3.4 Bias/control (BIAS) block

The bias/control block provides reference voltages and currents for all other circuit blocks (see Figure 3-4). An on-chip bandgap reference circuit provides the needed voltage and current references based on a programmable chip 6.19 KΩ ± 1% resistor.

Figure 3-4 Bias/control block diagram

Figure 3-5 and Figure 3-6 show the PMU block diagrams.

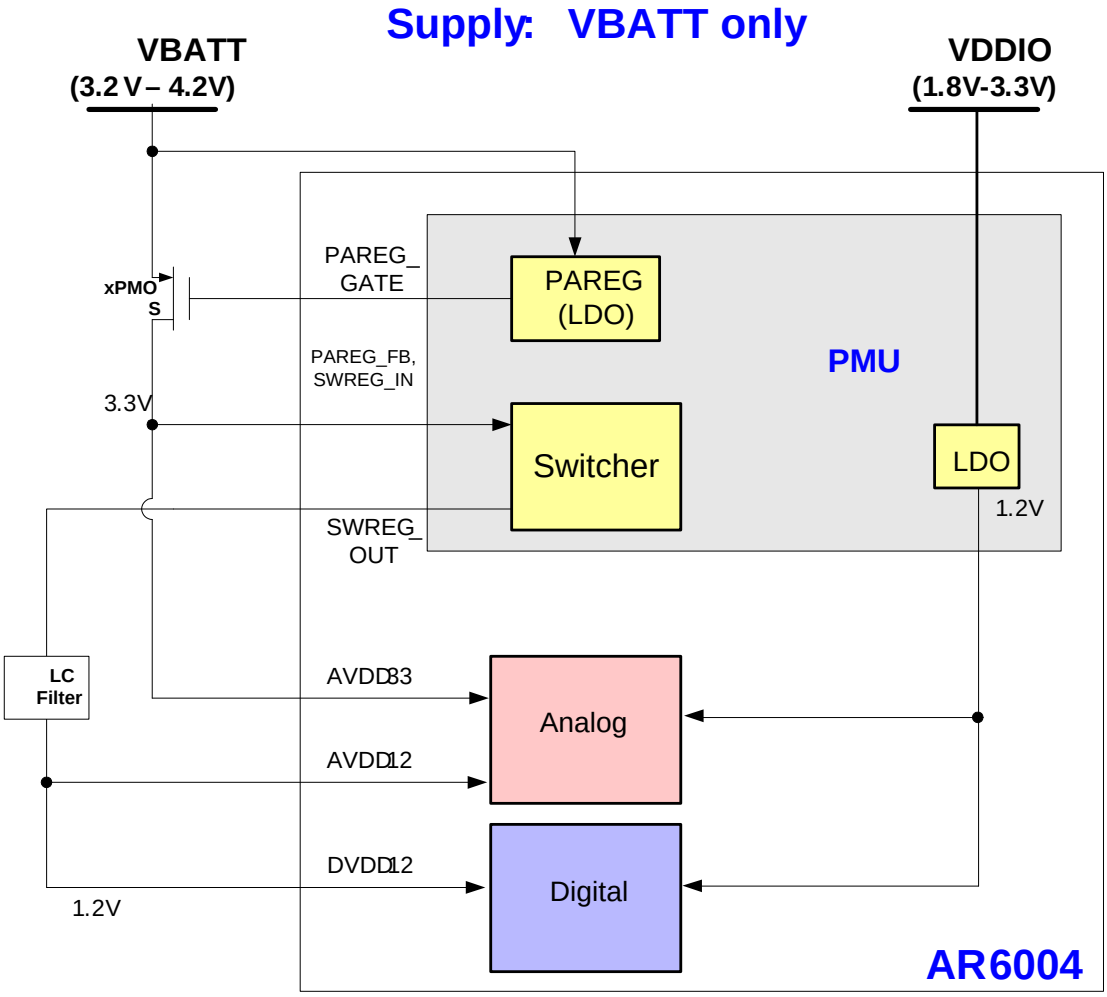

Figure 3-5 Direct connect to battery PMU block diagram

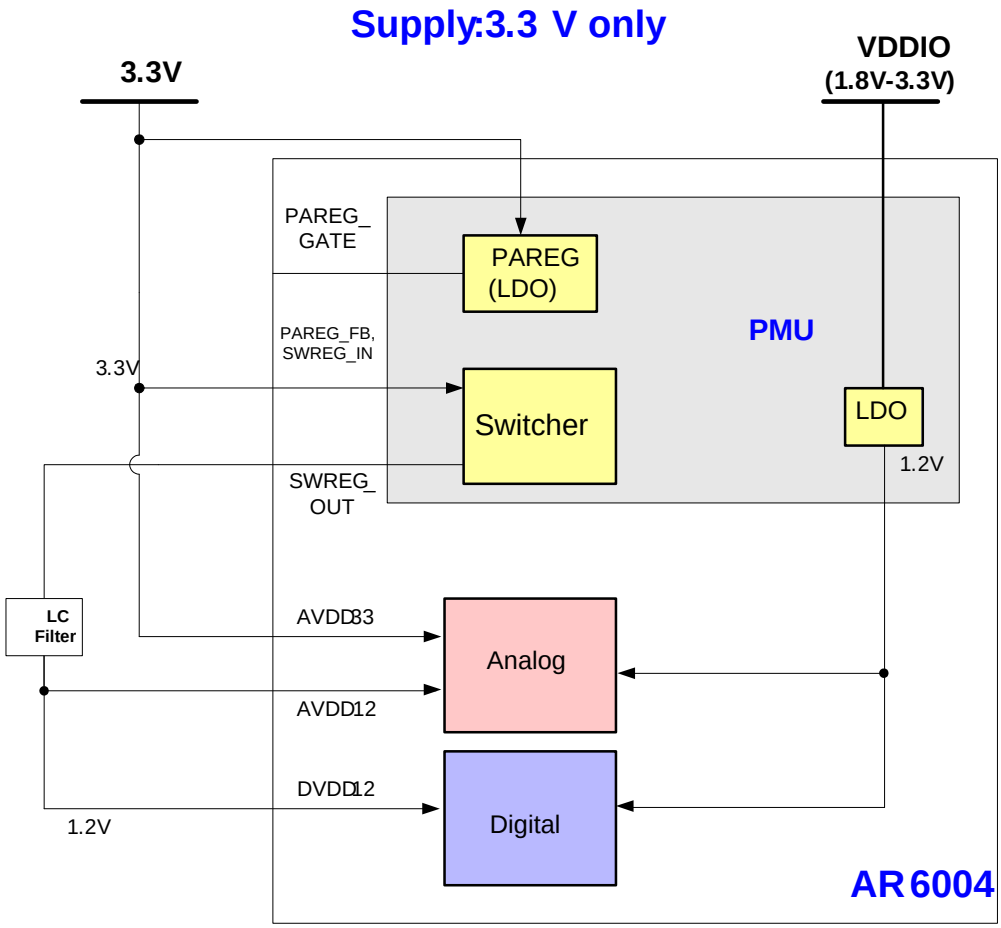

Figure 3-6 3.3 V input PMU block diagram

4 Electrical Characteristics

4.1 Absolute maximum ratings

Table 4-1 lists the absolute maximum ratings and Table 4-2 lists the recommended operating conditions for the AR6004. Absolute maximum ratings are those values beyond which damage to the device can occur.

Functional operation under these conditions, or at any other condition beyond those indicated in the operational sections of this document, is not recommended. Maximum rating for signals follows the supply domain of the signals.

Table 4-1 Absolute maximum ratings

Symbol (domain)	Parameter	Max rating	Unit
DVDD_GPIO1	I/O supply for GPIO1 pins	-0.3 to 4.0	V
DVDD_GPIO2	I/O supply for GPIO2 pins	-0.3 to 4.0	V
DVDD_GPIO3	I/O supply for GPIO3 pins	-0.3 to 4.0	V
DVDD_SDIO	Host interface I/O supply	-0.3 to 4.0	V
VDD33_ANT	Antenna control I/O supply	-0.3 to 4.0	V
VDD33_BB0/1	3.3 V supply for analog BBs	-0.3 to 4.0	V
VDD33_RF/1	3.3 V supply for analog RFs	-0.3 to 4.0	V
VDD33_SYNTH	3.3 V supply for analog SYNTH	-0.3 to 4.0	V
VDD33_PLL	3.3 V supply for analog PLL	-0.3 to 4.0	V
VDD33_USB	3.3 V supply for USB PHY	-0.3 to 4.0	V
PAREG_FB	External 3.3 V supply (N/A if PAREG is used)	-0.3 to 4.0	V
VDD33_XTAL	3.3 V supply for XTAL	-0.3 to 4.0	V
VBATTERY_42	External 3.3 V supply (if external supplies are used)	-0.3 to 4.2	V
	Battery voltage input (if internal PMU is used)		V
VDD12_BB0/1	1.2 V supply for analog BBs	-0.3 to 1.32	V

Symbol (domain)	Parameter	Max rating	Unit
VDD12_SYNTH	1.2 V supply for analog SYNTH	-0.3 to 1.32	V
VDD12_RF0/1	1.2 V supply for analog RFs	-0.3 to 1.32	V
VDD12_PLL	1.2 V supply for analog PLL	-0.3 to 1.32	V
VDD12_USBPLL	1.2 V supply for USB PLL	-0.3 to 1.32	V
DVDD12	Digital 1.2 V supply	-0.3 to 1.32	V
SWREG_IN	1.2 V switcher supply	3.65	V
RF_{in}	Maximum RF input (reference to 50-ohm input)	+10	dBm
T_{store}	Storage temperature	-45 to 135	°C
ESD	Electrostatic discharge tolerance	2000	V
3.3 V I/O VIH MAX	Maximum digital I/O input voltage for 3.3 V I/O supply	V_{dd} +0.3	V
VIH MIN	Minimum digital I/O input voltage for 1.8 V or 3.3 V I/O supply	-0.3	V

4.2 Recommended operating conditions

Table 4-2 lists the recommended operating conditions for the AR6004.

Table 4-2 Recommended operating conditions

Symbol (domain)	Parameter	Min	Typ	Max	Unit
DVDD_SDIO	Host interface I/O supply	1.71		3.46	V
DVDD_GPIO1/2/3	GPIO I/O supplies	1.71		3.46	V
VBATTERY_42	External 3.3 V supply (if external supplies are used)	3.14	3.3	3.46	V
	Battery voltage input (if internal PMU is used)	3.2		4.2	V
VDD33_ANT	Antenna control I/O supply	3.2	3.3	3.46	V
VDD33_BB0/1, VDD33_RF0/1, VDD33_SYNTH, VDD33_PLL, VDD33_USB, VDD33_XTAL	Analog 3.3 V supplies	3.14	3.3	3.46	V

Symbol (domain)	Parameter	Min	Typ	Max	Unit
VDD12_BB0/1, VDD12_SYNTH, VDD12_RF0/1, VDD12_PLL, VDD12_USB, VDD12_USBPLL	Analog 1.2 V supplies	1.20	1.26	1.32	V
DVDD12	Digital 1.2 V supply	1.20	1.26	1.32	V
SWERG_IN	1.2 V switcher supply	3.14	3.3	3.46	V
T_{case}	Case temperature		85		°C
Psi_{JT}	Junction to top center of the package thermal resistance		2.5		°C/W
$T_{ambient}$	Ambient temperature	-40		85	°C

4.3 DC electrical characteristics

Table 4-3 lists the general DC electrical characteristics over recommended operating conditions (unless otherwise specified).

Table 4-3 General DC electrical characteristics (for 3.3 V I/O operation)

Symbol	Parameter		Conditions	Min	Typ	Max	Unit
V_{IH}	High-level input voltage			0.7 x V_{dd}			V
V_{IL}	Low-level input voltage					0.3 x V_{dd}	V
I_{IL}	Input leakage current	Without pull-up or pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	0		-3	nA
		With pull-up	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	16		48	µA
		With pull-down	0 V < V_{in} < V_{dd} 0 V < V_{out} < V_{dd}	-14		-47	µA
V_{OH}	High-level output voltage		I_{oh} = -4mA	0.9 x V_{dd}			V
			I_{oh} = -12mA	0.9 x V_{dd}			V
V_{OL}	Low-level output voltage		I_{oh} = 4mA			0.1 x V_{dd}	V
			I_{oh} = 12mA			0.1 x V_{dd}	V

4.4 Radio receiver characteristics

Table 4-4 and Table 4-6 list the AR6004 receiver characteristics.

Table 4-4 Receiver characteristics for 2.4 GHz dual-chain operation

Symbol	Parameter	Conditions[1] [2]	Min	Typ[3]	Max	Unit
F_{rx}	Receive input frequency range		2.412		2.484	GHz
S_{rf}	Sensitivity					
	CCK, 1 Mb/s			-99		dBm
	CCK, 2 Mb/s			-96		
	CCK, 5.5 Mb/s			-93		
	CCK, 11 Mb/s			-90		
	OFDM, 6 Mb/s			-94		
	OFDM, 9 Mb/s			-93		
	OFDM, 12 Mb/s			-93		
	OFDM, 18 Mb/s			-91		
	OFDM, 24 Mb/s			-87		
	OFDM, 36 Mb/s			-84		
	OFDM, 48 Mb/s			-80		
	OFDM, 54 Mb/s			-78		
	HT20, MCS0			-94		
	HT20, MCS1			-91		
	HT20, MCS2			-89		
	HT20, MCS3			-87		
	HT20, MCS4			-85		
	HT20, MCS5			-80		
	HT20, MCS6			-79		
	HT20, MCS7			-77		

[1] Using LDPC improves the sensitivity of HT rates by 1 - 2 d

[2] In LPL mode, sensitivity will be degraded by 1 - 2 d

[3] Performance measured at the balu

Symbol	Parameter	Conditions[1] [2]	Min	Typ[3]	Max	Unit
	HT20, MCS8			-92		
	HT20, MCS9			-89		
	HT20, MCS10			-87		
	HT20, MCS11			-84		
	HT20, MCS12			-82		
	HT20, MCS13			-77		
	HT20, MCS14			-75		
	HT20, MCS15			-73		

Table 4-5 Adjacent channel rejection for 2.4 GHz dual-chain operation

Symbol	Parameter	Conditions [4]	Min	Typ	Max	Unit
radj	Adjacent channel rejection					
	CCK, 1 Mb/s			35		dB
	CCK, 11 Mb/s			35		
	OFDM, 6 Mb/s			32		
	OFDM, 54 Mb/s			16		
	HT20, MCS0			31		
	HT20, MCS7			14		
	HT20, MCS15			13		

Table 4-6 Receiver characteristics for 5 GHz dual chain operation

Symbol	Parameter	Conditions[5] [6] [7]	Min	Typ	Max	Unit
F_{rx}	Receive input frequency range		4.90		5.925	GHz
S_{rf}	Sensitivity					
	OFDM, 6 Mb/s			-93		dBm

[4] Performance measured at the balu
[5] Using LDPC improves the sensitivity of HT rates by 1 - 2 d
[6] In LPL mode, sensitivity will be degrade by 1 - 2 d
[7] Performance measured at the balu

Symbol	Parameter	Conditions[5 6 7]	Min	Typ	Max	Unit
	OFDM, 9 Mb/s			-92		
	OFDM, 12 Mb/s			-92		
	OFDM, 18 Mb/s			-90		
	OFDM, 24 Mb/s			-86		
	OFDM, 36 Mb/s			-83		
	OFDM, 48 Mb/s			-79		
	OFDM, 54 Mb/s			-77		
	HT20, MCS0			-93		
	HT20, MCS1			-90		
	HT20, MCS2			-88		
	HT20, MCS3			-85		
	HT20, MCS4			-83		
	HT20, MCS5			-78		
	HT20, MCS6			-76		
	HT20, MCS7			-74		
	HT20, MCS8			-91		
	HT20, MCS9			-88		
	HT20, MCS10			-86		
	HT20, MCS11			-82		
	HT20, MCS12			-80		
	HT20, MCS13			-73		
	HT20, MCS14			-72		
	HT20, MCS15			-71		
	HT40, MCS0			-90		
	HT40, MCS1			-87		
	HT40, MCS2			-85		
	HT40, MCS3			-82		

Symbol	Parameter	Conditions[5] [6] [7]	Min	Typ	Max	Unit
	HT40, MCS4			-79		
	HT40, MCS5			-74		
	HT40, MCS6			-73		
	HT40, MCS7			-70		
	HT40, MCS8			-87		
	HT40, MCS9			-84		
	HT40, MCS10			-81		
	HT40, MCS11			-78		
	HT40, MCS12			-74		
	HT40, MCS13			-70		
	HT40, MCS14			-68		
	HT40, MCS15			-67		

Table 4-7 Adjacent channel rejection for 5 GHz dual chain operation

Symbol	Parameter	Conditions[8]	Min	Typ	Max	Unit
R_{adj}	Adjacent channel rejection					
	OFDM, 6 Mb/s			22		dB
	OFDM, 54 Mb/s			9		
	HT20, MCS0			20		
	HT20, MCS7			19		
	HT20 MCS15			19		
	HT40, MCS0			18		
	HT40, MCS7			6		
	HT40, MCS15			4		

[8] Performance measured at the balu

4.5 Radio Tx characteristics

Table 4-8 and **Table 4-9** list the Tx characteristics for AR6004.

NOTE: The two-chain operation will provide 3 dB higher output than a single-chain operation listed in Table 4-8.

Table 4-8 Tx characteristics for 2.4 GHz per chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		2.412		2.484	GHz
Pout	Output power[9, 10]					
	11b mask compliant	1 Mb/s		20		dBm
	11g mask compliant	6 Mb/s		20		
	11g EVM compliant	54 Mb/s		18		
	11n HT20 mask compliant	MCS0		20		
	11n HT20 EVM compliant	MCS7		17		
	11n HT20 EVM compliant	MCS15		16		
Apc	Accuracy of power control			+1.5		dB

NOTE: The two-chain operation will provide 3dB higher output than a single chain operation listed in Table 4-9.

Table 4-9 Tx characteristics for 5 GHz per chain operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_{tx}	Transmit output frequency range		4.90		5.925	GHz
Pout	Output power[11]					
	11n HT20 mask compliant	MCS0		18.0		

[9] Refer to IEEE 802.11 specification for transmit spectrum limits:
- 802.11b mask (18.4.7.3)
- 802.11g mask (19.5.4)
- 802.11g EVM (17.3.9.6.3)
- 802.11n HT20 mask (20.3.21.1)
- 802.11n HT20 EVM (20.3.21.7.3)

[10] Performance measured at the balun.

[11] Performance measured at the balun.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
	11n HT40 mask compliant	MCS0		14.0		dBm
	11a mask compliant	6 Mb/s		17.0		
	11a EVM compliant	54 Mb/s		15.0		
	11n HT20 EVM compliant	MCS7		10.5		
	11n HT40 EVM compliant	MCS7		10.5		
	11n HT20 EVM compliant	MCS15		10.0		
	11n HT40 EVM compliant	MCS15		9.0		
Apc	Accuracy of power control			+2.0		dB

4.6 AR6004 synthesizer characteristics

Table 4-10 and Table 4-11 summarize the synthesizer characteristics for the AR6004.

Table 4-10 Synthesizer composite characteristics for 2.4 GHz operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_c	Center channel frequency	Center frequency at 5 MHz spacing	2.412		2.484	GHz
F_{ref}	Reference oscillator frequency	+20 ppm		26[12]		MHz
F_{step}	Frequency step size (at RF)			1		MHz

Table 4-11 Synthesizer composite characteristics for 5 GHz operation

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
F_c	Center channel frequency	Center frequency at 5 MHz spacing	4.90		5.925	GHz
F_{ref}	Reference oscillator frequency	+20 ppm		26[13]		MHz
F_{step}	Frequency step size (at RF)	13		5		MHz

[12] Other supported frequencies are: 19.2, 24, 26, 38.4, 40, and 52 MHz.

[13] 5 MHz channel spacing is for the 5.725 to 5.925 GHz band.

4.7 Typical power consumption performance

4.7.1 Measurement conditions for SDIO low-power states

- T_ambient = 25C
- All I/O pins except CHIP_PWD_L are maintained at their default polarities (I/Os without default internal pulls are pulled low) (see Table 4-12 and Table 4-13)

Table 4-12 AR6004 typical current consumption in SDIO mode – low-power states at 3.3 V operation

Mode	State	Typical current consumption, single chain	Typical current consumption, dual chain
Standby	CHIP_PWD	7 uA	
	HOST_OFF	50 uA	
	SLEEP	250 uA	
IEEE Power Save, 2.4 GHz[14]	DTIM=1	2.28	2.75 mA
	DTIM=3	1.02	1.14 mA
	DTIM=10	0.52	0.56 mA
IEEE Power Save, 5 GHz[15]	DTIM=1	1.33	1.43 mA
	DTIM=3	0.64	0.65 mA
	DTIM=10	0.40	0.41 mA

4.7.2 Measurement conditions for HSIC low-power states

Table 4-13 AR6004 typical current consumption in HSIC mode – low-power states at 3.3 V operation

Mode	State	Typical current consumption, single chain	Typical current consumption, dual chain
Standby	CHIP_PWD	7 uA	
	SLEEP/SUSPEND	400 uA	

[14] Measured on a WBGF10 reference board, using HT20 bandwidth and LP
[15] Measured on a WBGF10 reference board, using HT20 bandwidth and LP

Mode	State	Typical current consumption, single chain	Typical current consumption, dual chain
IEEE Power Save, 2.4 GHz[16]	DTIM=1	3.41	3.82 mA
	DTIM=3	1.46	1.59 mA
	DTIM=10	0.77	0.81 mA
IEEE Power Save, 5 GHz[17]	DTIM=1	1.68	1.78 mA
	DTIM=3	0.88	0.91 mA
	DTIM=5	0.60	0.61 mA

4.7.3 Measurement conditions for continuous receive [2.4 GHz operation]

Table 4-14 AR6004 typical current consumption [2.4 GHz operation] – continuous receive at 3.3 V operation

Mode/rate [Mb/s]	Average current consumption at 3.3 V, mA, single chain [18]	Average current consumption at 3.3 V, mA, dual chain[19]
	Chain 1	Chain 1 & 2
RX 1 Mb/s	65	77
RX 11 Mb/s	66	77
RX 54 Mb/s	69	81
RX HT20 MCS0	67	74
RX HT20 MCS7	69	83
RX HT20 MCS15	-	88
RX HT40 MCS0	79	100
RX HT40 MCS7	81	103
RX HT40 MCS15	-	110

- T_ambient = 25C

[16] Measured on a WBGF10 reference board, using HT20 bandwidth, LPL, and the interface suspended
[17] Measured on a WBGF10 reference board, using HT20 bandwidth, LPL, and the interface suspended
[18] Using LPL
[19] Using SDIO, in HSIC mode consumption will be 15 mA higher

4.7.4 Measurement conditions for continuous transmit [2.4 GHz operation]

Table 4-15 AR6004 typical current consumption [2.4 GHz operation] – continuous transmit at 3.3 V operation

Rate	dBm per chain	Typical current consumption single chain mA	Typical current consumption dual chain [20] mA
Tx 1 Mb/s	19.0	236	424
Tx 11 Mb/s	19.0	237	424
Tx 54 Mb/s	18.0	233	415
Tx HT20 MCS0	20.0	249	450
Tx HT20 MCS7	17.0	229	400

- T_ambient = 25C

4.7.5 Measurement conditions for continuous receive [5 GHz operation]

Table 4-16 AR6004 typical current consumption [5 GHz operation] – continuous receive at 3.3 V operation

Mode/rate [Mb/s]	Typical current at 3.3 V. mA, single chain[21]	Typical current at 3.3 V. mA, dual chain[22] [23]
	Chain 1	Chain 1 & 2
RX 54 Mb/s	75	82
RX HT20 MCS0	79	87
RX HT20 MCS7	81	89
RX HT20 MCS15	-	91
RX HT40 MCS0	91	105

[20] Using SDIO, in HSIC mode consumption will be 15 mA higher
[21] Using LP
[22] Using SDIO, in HSIC mode consumption will be 15 mA high
[23] Measured using AR6004 TCMD tool build 2024

Mode/rate [Mb/s]	Typical current at 3.3 V. mA, single chain[21]	Typical current at 3.3 V. mA, dual chain[22] [23]
RX HT40 MCS7	93	107
RX HT40 MCS15	-	115

- T_ambient = 25C

4.7.6 Measurement conditions for continuous transmit [5 GHz operation]

Table 4-17 AR6004 typical current consumption [5 GHz operation] – continuous transmit at 3.3 V operation per chain

Mode/rate [Mb/s]	Target output power per chain [dBm]	Typical current consumption at 3.3 V, [mA], single chain	Typical current consumption at 3.3 V, [mA], dual chain[24]
OFDM, 6 Mb/s	17.0	304	547
OFDM 54 Mb/s	15.0	298	538
HT20, MCS0	18.0	311	562
HT20, MCS7	10.5	272	490
HT40, MCS0	14.0	300	532
HT40, MCS7	10.5	273	489

- T_ambient = 25C

[24] Using SDIO, in HSIC mode consumption will be 15 mA higher

5 AC Specifications

5.1 External 19.2/24/26/38.4/40/52 MHz reference input clock timing

Figure 5-1 and Table 5-1 show the external 19.2/24/26/38.4/40/52 MHz reference input clock timing requirements.

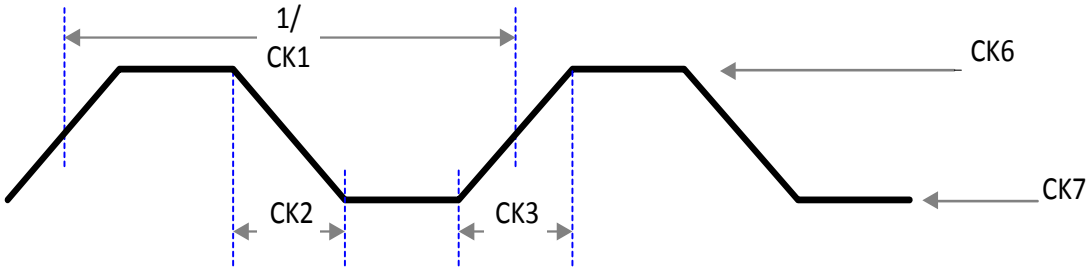

Figure 5-1 External 19.2/24/26/38.4/40/52 MHz

Table 5-1 External 19.2/24/26/38.4/40/52 MHz reference input clock timing

Symbol	Description	Min	Typ	Max	Unit
CK2	Fall time	-	-	0.1 x period	ns
CK3	Rise time	-	-	0.1 x period	ns
CK4	Duty cycle (high-to-low ratio)	40	-	60	%
CK5	Frequency stability	-20	-	20	ppm
CK6	Input high voltage	0.75		1.26	V
CK7	Input low voltage	-0.55		0.3	V

5.2 SDIO/GSPI interface timing

Figure 5-2 shows the SDIO timing. Figure 5-3 shows the write timing for GSPI style transactions.

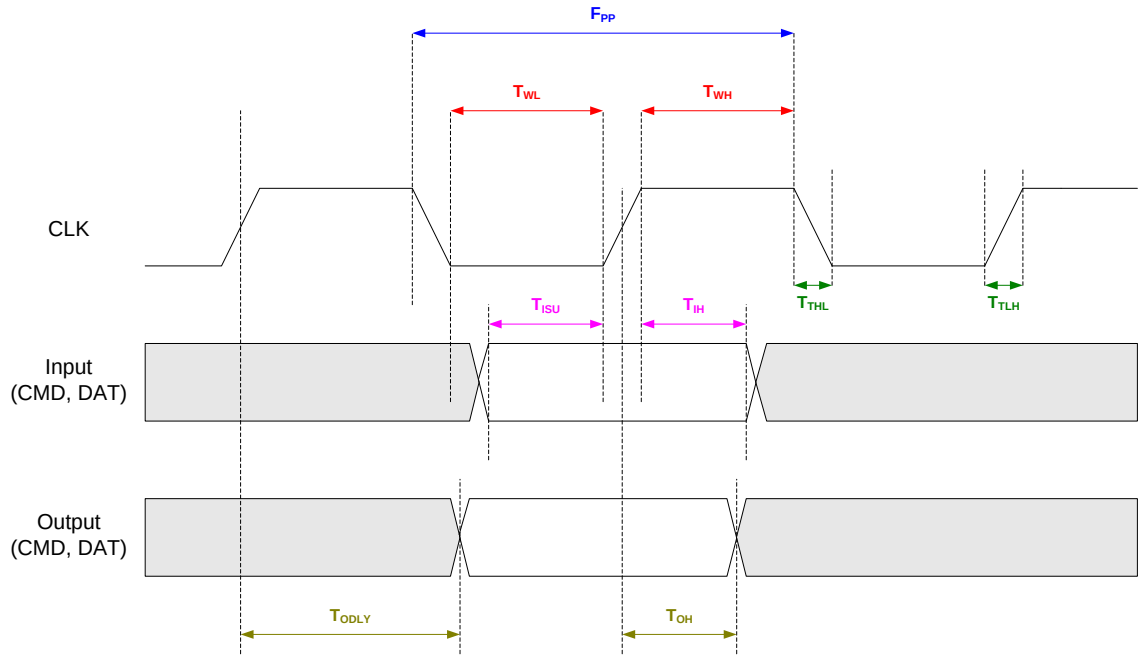

Figure 5-2 SDIO 2.0 timing

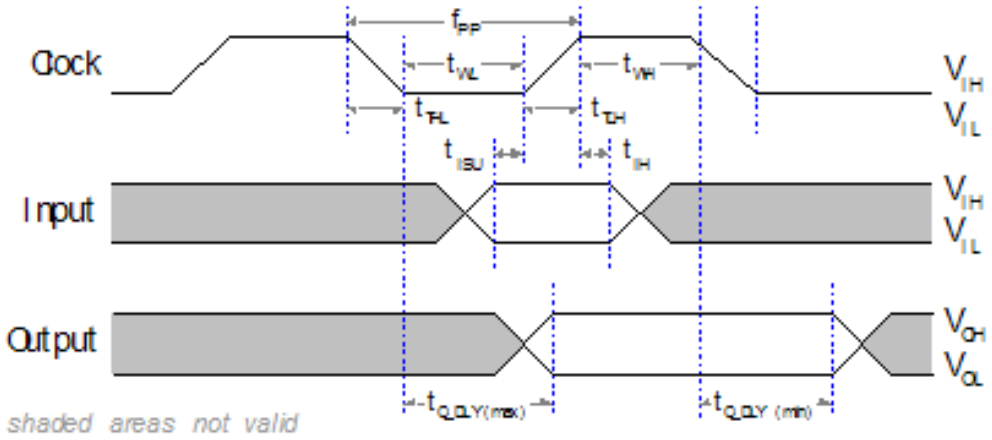

Figure 5-3 GSPI timing

Table 5-2 lists the values for timing constraints for SDIO.

Table 5-2 SDIO timing constraints

Parameter	Description	Min	Max	Unit	Note
f_{PP}	Clock frequency data transfer mode	0	50	MHz	40 pF ≥ C_L
t_{WL}	Clock low time	7	-	ns	40 pF ≥ C_L

Parameter	Description	Min	Max	Unit	Note
t_{WH}	Clock high time	7	-	ns	40 pF ≥ C_L
t_{TLH}	Clock rise time	-	10	ns	40 pF ≥ C_L
t_{THL}	Clock fall time	-	10	ns	40 pF ≥ C_L
t_{ISU}	Input setup time	6	-	ns	40 pF ≥ C_L
t_{IH}	Input hold time	2	-	ns	40 pF ≥ C_L
t_{OH}	Output hold time	2.5	-	ns	40 pF ≥ C_L
$t_{O\_DLY\ (min)}$	Output delay time during data transfer mode	0	14	ns	40 pF ≥ C_L

Table 5-3 lists the values for timing constraints for GSPI.

Table 5-3 GSPI timing constraints

Parameter	Description	Min	Max	Unit
f_{PP}	Clock frequency	0	48	MHz
t_{WL}	Clock low time	8.3	-	ns
t_{WH}	Clock high time	8.3	-	ns
t_{TLH}	Clock rise time	-	2	ns
t_{THL}	Clock fall time	-	2	ns
t_{ISU}	Input setup time	5	-	ns
t_{IH}	Input hold time	5	-	ns
t_{O_DLY}	Output delay	0	5	ns

6 Pin Descriptions

This section contains a listing of the signal descriptions (see Table 6-1 for the BGA package pin outs).

Table 6-1 lists the nomenclature used for signal names.

Table 6-1 Nomenclature for signal names

Term	Description
NC	No connection should be made to this pin
_L	At the end of the signal name, indicates active low signals
P	At the end of the signal name, indicates the positive side of a differential signal
N	At the end of the signal name indicates the negative side of a differential signal

Table 6-2 lists the nomenclature used for signal types.

Table 6-2 Nomenclature for signal types

Term	Description
IA	Analog input signal
I	Digital input signal
IO	Digital bidirectional signal
OA	An analog output signal
O	A digital output signal
P	A power or ground signal

AR6004	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	NC	GPIO_15	ANTD	ANTB	RFIN2P0	RFIN2N0	RFIN5N0	RFIN5P0	RF2OUTN0	RF2OUTP0	RF5OUTN0	RF5OUTP0	XPABIAS20	NC
B	GPIO_13	GPIO_14	VDD33_ANT	ANTC	ANTA	GND	GND	GND	GND	GND	GND	XPABIAS50	XPABIAS51	RFIN2P1
C	GPIO_11	GPIO_12											XPABIAS21	RFIN2N1
D	GPIO_9	GPIO_10		DVDD_GPIO1	GND	GND	VDD12_BB0		VDD12_RF0	VDD33_RF0	VDD33_SYNTH		GND	RFIN5N1
E	GPIO_7	GPIO_8			GND	GND	GND	GND		VDD12_SYNTH	VDD33_RF1		GND	RFIN5P1
F	GPIO_5	GPIO_6		GND	GND	GND	GND	GND	GND	VDD12_RF1	VDD33_PLL		GND	RF2OUTN1
G	GPIO_3	GPIO_4		SREG_OUT	GND	GND	GND	GND	VDD12_BB1		VDD12_PLL		GND	RF2OUTP1
H	GPIO_1	GPIO_2		DVDD_SDIO	GND	GND	GND	GND	GND	GND	GND		GND	RF5OUTN1
J	CHIP_PWD_L	GPIO_0			GND	GND	GND	GND	GND	GND	GND		GND	RF5OUTP1
K	DVDD12	DVDD12		SWREG_GND	SWREG_GND	GND	GND	GND	GND	GND	GND		GND	VDD33_XTAL
L	SWREG_OUT	SWREG_OUT		SWREG_GND	SWREG_GND	GND	GND	DVDD_GPIO3	GND	GND	DVDD_GPIO2		GND	XTALI
M	SWREG_IN	SWREG_IN											GND	XTALO
N	SWREG_IN	PAREG_FB	VDD33_USB	VDD12_USB	VDD12_USBPL	DVDD12	GPIO_49	GPIO_47	GPIO_45	GPIO_43	GPIO_41	GPIO_39	GPIO_35	EXT_CLK_OUT
P	NC	PAREG_GATE	VBATT_VDD3	HSIC_DATA	HSIC_STROBE	DVDD12	GPIO_50	GPIO_46	GPIO_44	GPIO_42	GPIO_40	GPIO_37	GPIO_36	NC

Figure 6-1 BGA package pinout

Table 6-3 lists the signal and pin descriptions.

Table 6-3 Signal to pin mapping

Pin no.	Name	Type	I/O level	Description
K1, K2, N6, P6	DVDD12	Supply1.2V	1.26 V	Core 1.2 V supply
L8	DVDD_GPIO3	I/O Supply	1.8 - 3.6 V	I/O supply for GPIOs 44 - 47, 49-50
L11	DVDD_GPIO2	I/O Supply	1.8 - 3.6 V	I/O supply for GPIOs 35 - 38, 40 - 43
D4	DVDD_GPIO1	I/O Supply	1.8 - 3.6 V	I/O supply for GPIOs 12 - 15
H4	DVDD_SDIO	I/O Supply	1.8 - 3.6 V	I/O supply for GPIOs 0 - 11
A1, A14, P1, P14	NC	NC	-	Not connected
P7	GPIO50	Digital I/O	DVDD_GPIO3	GPIOs
N7	GPIO49	Digital I/O	DVDD_GPIO3	

Pin no.	Name	Type	I/O level	Description
N8	GPIO47	Digital I/O	DVDD_GPIO3	
P8	GPIO46	Digital I/O	DVDD_GPIO3	
N9	GPIO45	Digital I/O	DVDD_GPIO3	
P9	GPIO44	Digital I/O	DVDD_GPIO3	
N10	GPIO43	Digital I/O	DVDD_GPIO2	
P10	GPIO42	Digital I/O	DVDD_GPIO2	
N11	GPIO41	Digital I/O	DVDD_GPIO2	
P11	GPIO40	Digital I/O	DVDD_GPIO2	
N12	GPIO38	Digital I/O	DVDD_GPIO2	
P12	GPIO37	Digital I/O	DVDD_GPIO2	
P13	GPIO36	Digital I/O	DVDD_GPIO2	
N13	GPIO35	Digital I/O	DVDD_GPIO2	
A2	GPIO15	Digital I/O	DVDD_GPIO1	
B2	GPIO14	Digital I/O	DVDD_GPIO1	
B1	GPIO13	Digital I/O	DVDD_GPIO1	
C2	GPIO12	Digital I/O	DVDD_GPIO1	
C1	GPIO11	Digital I/O	DVDD_SDIO	
D2	GPIO10	Digital I/O	DVDD_SDIO	
D1	GPIO9	Digital I/O	DVDD_SDIO	
E2	GPIO8	Digital I/O	DVDD_SDIO	
E1	GPIO7	Digital I/O	DVDD_SDIO	
F2	GPIO6	Digital I/O	DVDD_SDIO	
F1	GPIO5	Digital I/O	DVDD_SDIO	SDIO_CLK/GPIO
G2	GPIO4	Digital I/O	DVDD_SDIO	SDIO_D0/GPIO
G1	GPIO3	Digital I/O	DVDD_SDIO	SDIO_D1/GPIO
H2	GPIO2	Digital I/O	DVDD_SDIO	SDIO_D2/GPIO
H1	GPIO1	Digital I/O	DVDD_SDIO	SDIO_D3/GPIO

Pin no.	Name	Type	I/O level	Description
J2	GPIO0	Digital I/O	DVDD_SDIO	SDIO_CMD/GPIO
J1	CHIP_PWD_L	Digital Input	DVDD_SDIO	Reset signal to power down the AR6004 (Active low)
P4	HSIC_DATA	IOA		HSIC data
P5	HSIC_STROBE	IOA		HSIC strobe
L1, L2	SWREG_OUT	-	-	Connect an LC filter: L in series with (L1, L2) and (K1, K2) C in parallel with (K1, K2) to SWREG_GND
M1, M2, N1	SWREG_IN	3.3 V Input	-	Connect to 3.3 V supply
K4, K5, L5, L4	SWREG_GND	GND	GND	Switching regulator ground
N2	PAREG_FB	I	3.3 V	PAREG feedback input
P2	PAREG_GATE	O	3.3 V	PAREG gate control output
G4	SREG_OUT	O	1.2 V	Connect to external 470pF capacitor
A3	ANTD	O	3.3 V	Control signal for RF front end
B4	ANTC	O	3.3 V	Control signal for RF front end
A4	ANTB	O	3.3 V	Control signal for RF front end
B5	ANTA	O	3.3 V	Control signal for RF front end
B3	VDD33_ANT	I	3.3 V	I/O supply for RF front end controls
N3	VDD33_USB	I	3.3 V	3.3 V supply for USB PHY
E11	VDD33_RF1	I	3.3 V	3.3 V supply for chain 1 PA
D10	VDD33_RF0	I	3.3 V	3.3 V supply for chain 0 PA
F11	VDD33_PLL	I	3.3 V	3.3 V supply for internal PLL
D11	VDD33_SYNTH	I	3.3 V	3.3 V supply for internal synthesizer
K14	VDD33_XTAL	I	3.3 V	3.3 V supply for internal oscillator
N4	VDD12_USB	I	1.2 V	1.2 V supply for USB PHY
N5	VDD12_USBPL	I	1.2 V	1.2 V supply for USB PLL

Pin no.	Name	Type	I/O level	Description
E10	VDD12_SYNTH	I	1.2 V	1.2 V supply for internal synthesizer
F10	VDD12_RFI	I	1.2 V	1.2 V supply for chain 1 PA
D9	VDD12_RF0	I	1.2 V	1.2 V supply for chain 0 PA
G9	VDD12_BB1	I	1.2 V	1.2 V supply for analog baseband
D7	VDD12_BB0	I	1.2 V	1.2 V supply for analog baseband
G11	VDD12_PLL	I	1.2 V	1.2 V supply for internal PLL
P3	VBATT_VDD33	I	2.8 V - 4.2 V	Battery input
N14	EXT_CLK_OUT	O	1.2 V	Reference clock output to external chip
M14	XTALO			Reference crystal interface signal or external reference clock input
L14	XTALI			Reference clock interface signal
A5	RFIN2P0	IA		2.4 GHz RF input
A6	RFIN2N0	IA		2.4 GHz RF input
A7	RFIN5N0	IA		5 GHz RF input
A8	RFIN5P0	IA		5 GHz RF input
A9	RF2OUTN0	OA		2.4 GHz RF output
A10	RF2OUTP0	OA		2.4 GHz RF output
A11	RF5OUTN0	OA		5 GHz RF output
A12	RF5OUTP0	OA		5 GHz RF output
B14	RFIN2P1	IA		2.4 GHz RF input
C14	RFIN2N1	IA		2.4 GHz RF input
D14	RFIN5N1	IA		5 GHz RF input
E14	RFIN5P1	IA		5 GHz RF input
F14	RF2OUTN1	OA		2.4 GHz RF output
G14	RF2OUTP1	OA		2.4 GHz RF output
H14	RF5OUTN1	OA		5 GHz RF output

Pin no.	Name	Type	I/O level	Description
J14	RF5OUTP1	OA		5 GHz RF output
P4	HSIC_DATA	IOA		HSIC data
P5	HSIC_STROBE	IOA		HSIC strobe
A13	XPABIAS20	OA		Bias voltage for first optional 2.4 GHz external PA
B12	XPABIAS50	OA		Bias voltage for first optional 5 GHz external PA.
C13	XPABIAS21	OA		Bias voltage for second optional 2.4 GHz external PA.
B13	XPABIAS51	OA		Bias voltage for second optional 5 GHz external PA.
B6, B7, B8, B9, B10, B11, D5, D6, D13, E5, E6, E7, E8, E13, F4, F5, F6, F7, F8, F9, F13, G5, G6, G7, G8, G13, H5, H6, H7, H8, H9, H10, H11, H13, J5, J6, J7, J8, J9, J10, J11, J13, K6, K7, K8, K9, K10, K11, K13, L6, L7, L9, L10, L13, M13	GND	-	-	Analog/Digital ground

7 Package Dimensions

7.1 BGA dimensions

The BGA drawing and measurements are provided in Figure 7-1. Also see Table 7-1 for BGA dimensions.

- 6 x6 mm, 0.4 mm pitch BGA-155, or
- 0.2 mm pitch WLCSP package information available separately

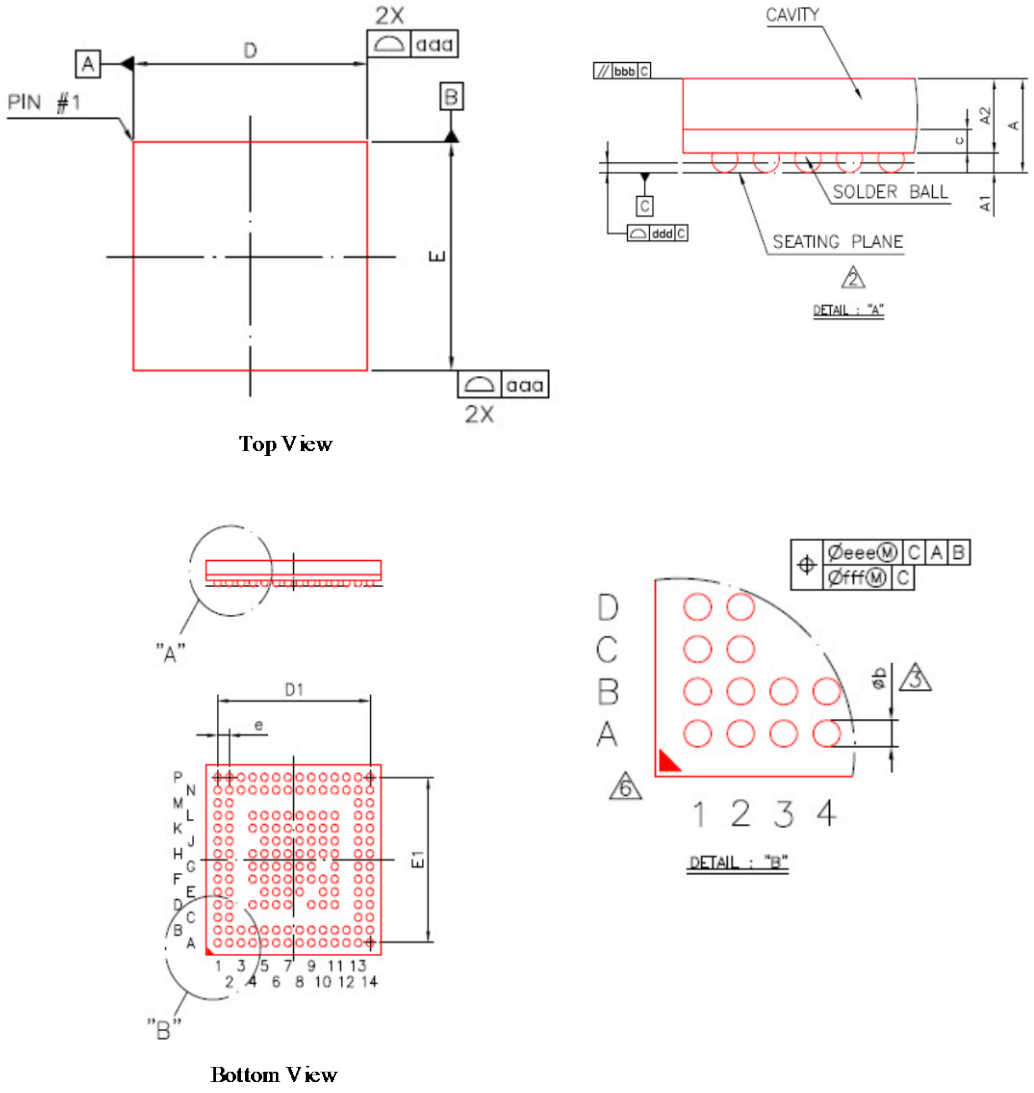

Figure 7-1 BGA drawing 6 x 6 mm package

Table 7-1 BGA dimensions

Dimension label	Min	Nom	Max	Unit	Min	Nom	Max	Unit
A	---	---	1.00	mm	---	---	0.039	inches
A1	0.13	0.18	0.23	mm	0.005	0.007	0.009	inches
A2	0.61	0.66	0.71	mm	0.024	0.026	0.028	inches
c	0.17	0.21	0.25	mm	0.007	0.008	0.010	inches
D	5.90	6.00	6.10	mm	0.232	0.236	0.240	inches
E	5.90	6.00	6.10	mm	0.232	0.236	0.240	inches
D1	---	5.20	---	mm	---	0.205	---	inches
E1	---	5.20	---	mm	---	0.205	---	inches
e	---	0.40	---	mm	---	0.016	---	inches
b	0.20	0.25	0.30	mm	0.008	0.010	0.012	inches
aaa	0.10			mm	0.004			inches
bbb	0.10			mm	0.004			inches
ddd	0.08			mm	0.003			inches
eee	0.15			mm	0.006			inches
fff	0.05			mm	0.002			inches
MD/ME	14/14			mm	14/14			inches

Notes:

1. Controlling dimension: Millimeters.
2. Minimum clearance of 0.25 mm between edge of solder ball and body edge.

8 Ordering Information

The AR6004 may be ordered as follows:

- AR6004G-AC3D (2.4 GHz, BGA)
- AR6004G-AC3D-R (2.4 GHz, BGA, T&R)
- QCA6018G-AF1D-R (2.4 GHz, CSP, T&R)
- AR6004X-AC3D (5 GHz, BGA)
- AR6004X-AC3D-R (5 GHz, BGA, T&R)
- QCA6018X-AF1D-R (5 GHz, CSP, T&R)
- AR6004G-BC3D (2.4 GHz, BGA)
- AR6004G-BC3D-R (2.4 GHz, BGA, T&R)
- QCA6018G-BF1D-R (2.4 GHz, CSP, T&R)
- AR6004X-BC3D (5 GHz, BGA)
- AR6004X-BC3D-R (5 GHz, BGA, T&R)
- QCA6018X-BF1D-R (5 GHz, CSP, T&R)

A Terms and Acronyms

Table A-1 Acronyms, abbreviations, and terms

Term	Definition
AES	Advanced encryption standard
AHB	Advanced high-performance bus
APB	Advanced peripheral bus
BB	Baseband module
BGA	Ball grid arrays
BIAS	Associated bias/control
BT	Bluetooth
DAC	Digital to analog converters
DCU	DCF control unit
DRU	DMA receive unit
EPA	Efficient power amplifier
EVA	Error vector magnitude
GPIO	General-purpose input/output
HCI	Host controller interface
HIU	Host interface unit
HLS	Hybrid location system
I2C	Inter-integrated circuit
IF	Intermediate frequency
I/Q	In-phase/quadrature-phase
JTAG	Joint Test Action Group (ANSI/ICEEE Std. 1149.1-1760)
LDPC	Low-density parity check
LNA	Low-noise amplifier
LO	Local oscillator
LPL	Low-power listen
ML	Maximum likelihood
MRC	Maximum ratio combining
MSDU	MAC service data units
PA	Power amplifier
PCU	Protocol control unit
PHY	Physical layer
PIF	Peripheral interface
PLL	Phase-locked loop
PMU	Power management unit

Term	Definition
PTA	Packet traffic arbitration
PWM	Pulse-width modulation
QCU	Queue control unit
QOS	Quality of service
RF	Radio frequency
RIFS	Reduced inter-frame spacing
RTC	Real time clock
RTT	Round trip time
Rx	Receiver
SI	Serial interface
SPI	Serial peripheral interface
STBC	Space time block coding
SYNTH	Frequency synthesizer
TKIP	Temporal key integrity protocol
Tx	Transmitter
TxBF	Transmit beamforming
UART	Universal asynchronous receiver/transmitter
VCO	Voltage controlled oscillator
VGA	Variable gain amplifier
WAPI	WLAN authentication and privacy infrastructure
WEP	Wired equivalent privacy
WLCSP	Wafer level chip scale packages
WMM	Wi-Fi multimedia

B EXHIBIT 1

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