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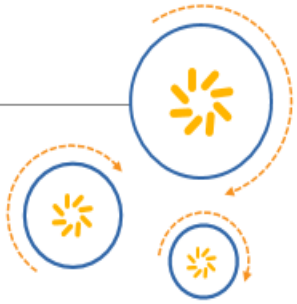

WCD9311 Audio Codec

Device Specification

September 2016

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LM80-P0598-3 Rev. B

Revision history

Revision	Date	Description
A	June 1, 2015	Initial release
B	September 23, 2016	Updated to E part

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Tables

1 Introduction

1.1 Documentation overview

This document provides a description of chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE Enabling some features may require additional licensing fees.

Technical information for the WCD9311 IC is primarily covered by the documents listed in Table 1-1, and all should be studied for a thorough understanding of the device and its applications.

Table 1-1 Primary WCD9311 documentation

Document	Title/description
WCD9311 Device Specification (this document)	Conveys all WCD9311 IC electrical and mechanical specifications. Additional material includes pin assignments; shipping, storage, and handling instructions; PCB mounting guidelines; and part reliability. This document can be used by company purchasing departments to facilitate procurement.
APQ8064E Chipset Data Sheet	Provides guidelines for the APQ8064E audio module, including a comprehensive overview of the WCD9311 audio codec IC.
I²C Bus Specification, version 2.1, January 2000	Philips Semiconductor document number 9398 393 40011.This document can be found at http://i2c2p.twibright.com/spec/i2c.pdf
I²S Bus Specification, version 2.1, February 1986	Philips Semiconductor *²S Bus Specification*,document.This document can be found at https://www.sparkfun.com/datasheets/BreakoutBoards/I2SBUS.pdf.
SLIMbus Specification	Serial Low-power Inter-chip Media Bus (SLIMbus) Specification. See http://www.mipi.org/specifications/serial-low-power-inter-chip-media-bus-slimbussm-specification

This WCD9311 device specification is organized as follows:

Chapter 1 Provides an overview of the WCD9311 documentation, gives a high-level functional description of the device, lists the device features, and defines marking conventions used throughout this document.

Chapter 2 Defines the device pin assignments.

Chapter 3 Defines the device electrical performance specifications, including absolute maximum and recommended operating conditions.

Chapter 4 Provides IC mechanical information, including dimensions, markings, ordering information, moisture sensitivity, and thermal characteristics.

Chapter 5 Discusses shipping, storage, and handling of the WCD9311 devices.

Chapter 6 Presents procedures and specifications for mounting the WCD9311 device onto printed circuit boards (PCBs).

Chapter 7 Presents WCD9311 device reliability data, including a definition of the qualification samples and a summary of qualification test results.

Appendix A Defines the terms and acronym used in this document

Appendix B Provides the terms of Exhibit 1.

1.2 WCD9311 device introduction

The WCD9311 IC is a standalone audio codec IC that supports multimedia solutions, including the APQ8064E chipset. Key WCD9311 functions include:

- Serial low-power inter-chip media bus (SLIMbus) for access to on-chip digital audio channels with fewer pins relative to inter-IC sound (I^2S) bus
- Seven analog input ports and eight analog output ports
- Seven analog-to-digital converters (ADCs) and eight digital-to-analog converters (DACs)
- Six digital microphone inputs (three clock/data pairs)
- Sidetone sample rate converter and infinite impulse response (IIR) filters for better performance and lower latency

The WCD9311 IC supports two I/O operating modes: SLIMbus and I^2S (selected using a dedicated hardware mode control pin). SLIMbus is the primary mode that provides access to all the audio codec paths and features, while I^2S provides access to fewer paths but maintains compatibility with earlier generation ICs. An example WCD9311 application is shown in Figure 1-1; this example uses the APQ8064E chipset with the primary WCD/APQ interface implemented via SLIMbus.

This highly integrated IC is very small – it uses the 6.0 × 6.0 × 1.27 mm, 86 pin chip-scale package (86 CSP) – and is supplemented by IC processing (such as the APQ8064E IC) to create an audio solution that reduces part count and PCB area. Companion chipsets ensure hardware and software compatibility to simplify the design cycle and reduce OEM time-to-market.

The WCD9311 IC uses low-power 65 nm CMOS fabrication technology, making it perfectly suited for battery-operated devices where power consumption and performance are critical.

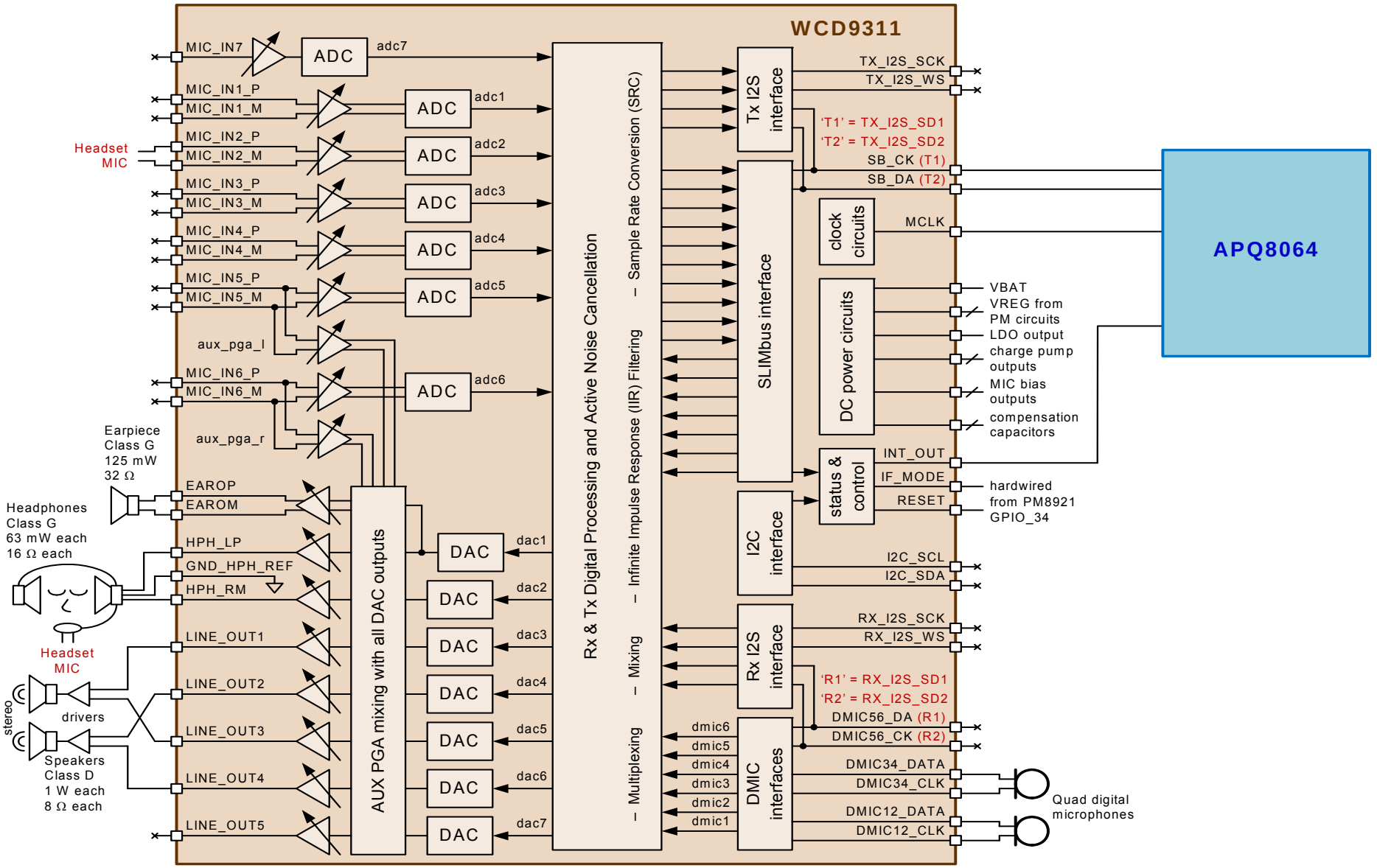


Figure 1-1 WCD9311 IC in a typical application

1.3 WCD9311 features

NOTE Some of the hardware features integrated within the WCD9311 IC must be enabled by software. Please see the latest version of the applicable software release notes to identify the enabled features.

1.3.1 Tx processing features

- Seven analog MIC input ports – six support differential and single-ended configurations, and one supports single-ended-only for the multibutton headset control (MBHC) feature
- Seven ADCs, one for each analog input
- MBHC with dedicated input to the ADC
  - Insertion/removal detection
  - Impedance (mic presence detection)
  - Detection for up to eight buttons
- Six digital microphone inputs with three clock lines, one for every digital microphone (DMIC) pair
- Ten concurrent Tx paths in SLIMbus mode
- 100 dB signal-to-noise ratio (SNR) (minimum) with 2.2 V analog supply and 0 dB gain mode
- SLIMbus interface that supports resolutions of 12, 16, 20, and 24 bits
- Input programmable gain settings of 0, 6, 12, and 18 dB
- Capless inputs (direct DC-coupled microphone support) and legacy capacitor-coupled inputs support
- Fixed input impedance of 10 k per pin (independent of amplifier gain) in input capacitor-coupled mode
- Four microphone bias circuits that can be used to power analog and DMICs
- Three independent pulse-code modulation (PCM) rates to support voice, music, and ultrasonic rates concurrently
- ANC path that is selectable from any ADC or digital microphone
- Digital gain control from -80 to +40 dB in 0.5 dB increments, plus mute
- Digital DC blocking filter with a selectable corner frequency of 3, 75, or 150 Hz
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz 2 mW stereo record at 48 kHz sample rate

NOTE The terms Rx and Tx refer to the flow of audio information with respect to a complete platform. For example, signals from a microphone to the WCD9311 are considered Tx path signals since the platform will transmit this information to the network.

1.3.2 Rx processing features

- Eight analog outputs – earpiece, headphone left and right, and five line outputs
- Dynamic range enhancement (DRE) for HPH and line-out power amplifiers (PAs)
- Eight DACs and seven interpolation paths (earpiece and headphone-left share one DAC path)
- Seven concurrent Rx paths
- 110 dB (typical) headphone SNR
- SLIMbus interface that supports resolutions of 12, 16, 20, and 24 bits in isochronous mode
- Differential earpiece output
  - Class G, 125 mW into 32 Ω
- Stereo single-ended headphone outputs (16 or 32 Ω)
  - Capless, class G, 63 mW into 16 Ω (each)
- Five single-ended line outputs (600 Ω)
  - Four can be used as stereo differential
- Adjustable headphone and line output gain settings
- Auxiliary programmable gain amplifier (PGA) to DAC PA mixing on all analog outputs, plus stereo to mono mixing
- Digital mixing at the input of each DAC path
- Three independent PCM rates to support voice, music, and ultrasonic rates concurrently
- 4 mW stereo playback at a 48 kHz sample rate
- Sample rates of 8, 16, 32, 48, 96, and 192 kHz
- Over-current protection on headphone and earpiece outputs
- Click and pop suppression
  - -80 dBVpp A-weighted (maximum) on the headphone outputs
  - -60 dBVpp A-weighted (maximum) on earpiece and line outputs

1.3.3 Additional processing and paths

- ANC supports feedforward, feedback, and adaptive modes
- Two sidetone paths with processing
  - All mixed channels operate at the same sample rate
  - No gain changes occur as a result of mixing channels
  - Two five-stage IIR filters
  - Two sample-rate converters
- Two auxiliary PGAs
  - Connected to inputs 5 and 6
  - Mixing with all DAC paths
  - Independent gain (-42 to +12 dB in 1.5 dB steps) with zero-crossing detection

1.3.4 Support features

- DC power management
  - LDO generates 1.95, 2.35, 2.75, and 2.85 V for internal microphone bias circuits
  - Charge pump generates plus and minus voltages
  - Supply gating and distribution to all other blocks
- Clock circuits
  - Master clocks supported: 24.576, 19.2, 12.288, and 9.6 MHz
  - Clock buffering, gating, and distribution to all other blocks
- Digital data, status, and control
  - Dedicated over-current protection interrupt
  - SLIMbus
    - 2-line bus that supports seven Rx inputs and ten Tx outputs, plus framer
    - Input and output mixing with flexible selection of routing signal paths
  - Inter-integrated circuit (I^2C) provides the legacy control interface
    - Fast-speed (400 kbps) mode
- Integrated IEC electrostatic discharge (ESD) (8 kV contact)

1.3.5 Package and other features

- Small package – 6 × 6 × 1.27 mm, 86 CSP, 0.5 mm pitch
- Many ground pins for improved electrical grounding, mechanical strength, and thermal continuity
- 65 nm CMOS technology
- Few external components required
- Pb-free, BrCl-free, RoHS compliant, SAC405 compliant

1.3.6 Summary of key WCD9311 features

Table 1-2 Key WCD9311 features

Feature	WCD9311 IC capability
System	
Highly integrated	More functionality, lower parts count, and less PCB area overall
Efficient	Lower power consumption
Tx processing	
Analog input ports and ADCs	Six of each, supporting differential and single-ended configurations Plus one single-ended microphone input and its ADC
Digital input ports	Six digital microphone inputs with three clock lines, one for every DMIC pair
Concurrency	Ten concurrent Tx paths
High dynamic range	100 dB SNR (minimum – 2.2 V supply and 0 dB gain)
Microphone biasing	Four voltage sources for powering analog and digital microphones MBHC and capless inputs support
ANC	Selectable from any ADC or digital microphone
Multiple sample rates	8, 16, 32, 48, 96, and 192 kHz
Concurrent PCM rates	Three independent rates support voice, music, and ultrasonic concurrently
Rx processing	
Analog output ports and DACs	Eight outputs – earpiece, headphone left and right, and five line outputs Eight DACs (earpiece and headphone left share one DAC path)
Wide variety of analog configurations	Differential earpiece output; class G, 125 mW into 32 Ω Stereo single-ended headphone outputs; capless, class G, 63 mW into 16 Ω (each) Five single-ended line outputs (600 Ω); four can be stereo differential
Concurrency	Seven concurrent Rx paths
High dynamic range	110 dB (typical) headphone SNR
Mixing	Auxiliary PGA to DAC PA mixing on all analog outputs; stereo to mono Digital mixing at the input of each DAC path
Protection and suppression	Over-current protection on headphone and earpiece outputs Click and pop suppression
Multiple sample rates	8, 16, 32, 48, 96, and 192 kHz

Table 1-2 Key WCD9311 features (cont.)

Feature	WCD9311 IC capability
Concurrent PCM rates	Three independent rates support voice, music, and ultrasonic concurrently
Additional processing and paths	
ANC	ANC supports feedforward, feedback, and adaptive modes
Sidetone paths and processing	All mixed channels operate at the same sample rate No gain changes occur as a result of mixing channels Two five-stage IIR filters Two sample-rate converters
Two auxiliary PGAs	Mixing with all DAC paths Independent gain with zero-crossing detection
Analog and digital support circuits	
DC power management	LDO generates 1.95, 2.35, 2.75, or 2.85 V for microphone bias circuits Charge pump generates plus and minus voltages Supply gating and distribution to all other blocks
Clock circuits	Master clocks supported: 24.576, 19.2, 12.288, and 9.6 MHz Clock buffering, gating, and distribution to all other blocks
Digital data, status, and control	Over-current protection interrupt SLIMbus – 2-line bus supports seven Rx inputs, ten Tx outputs, plus framer Input and output mixing with flexible selection of routing signal paths I^2C – supports 400 kHz fast-speed mode
Fabrication technology and package	
Single die	65 nm CMOS
Small, thermally efficient package	86 CSP: 6 × 6 × 1.27 mm, 0.5 mm pitch

1.4 Special marks

Table 1-3 defines special marks used in this document.

Table 1-3 Special marks

Mark	Definition
[ ]	Brackets ([ ]) sometimes follow a pin, register, or bit name. These brackets enclose a range of numbers. For example, DATA[7:4] may indicate a range that is 4 bits in length, or DATA[7:0] may refer to all eight DATA pins.
_N	A suffix of _N indicates an active low signal. For example, RESET_N.
0x0000	Hexadecimal numbers are identified with an x in the number, for example, 0x0000. All numbers are decimal (base 10) unless otherwise specified. Non-obvious binary numbers have the term binary enclosed in parentheses at the end of the number, for example, 0011 (binary).

2 Pin Definitions

The highly integrated WCD9311 device is available in the 86 pin CSP that includes several ground pins for electrical grounding, mechanical strength, and thermal continuity. See Chapter 4 for package details. A high-level view of the pin assignments is shown in Figure 2-1.

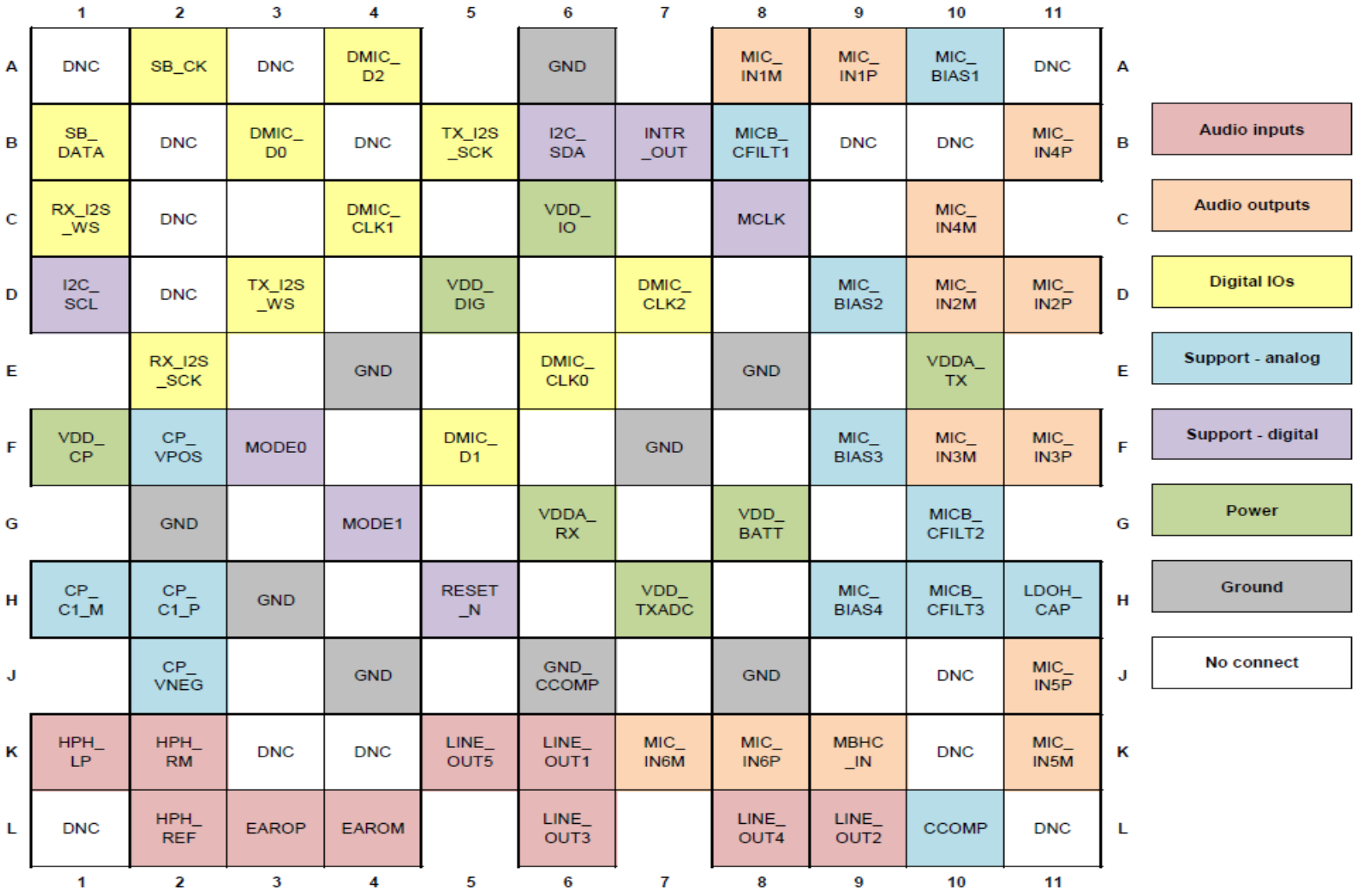


Figure 2-1 WCD9311 IC pin assignments (top view)

2.1 I/O parameter definitions

Table 2-1 I/O description (pad type) parameters

Symbol	Description
Pad attribute	
AI	Analog input (does not include pad circuitry)
AO	Analog output (does not include pad circuitry)
B	Bidirectional digital with CMOS input
DI	Digital input (CMOS)
DO	Digital output (CMOS)
Z	High-impedance (high-Z) output
Pad voltages for digital I/Os	
DIO	Digital I/Os supply (VDD_IO = 1.8 V)

2.2 Pin descriptions

Descriptions of all pins are presented in the following tables, organized by functional group:

Table 2-2 Analog outputs and Rx processing

Table 2-3 Analog inputs and Tx processing

Table 2-4 Digital data I/Os

Table 2-5 Support functions (analog)

Table 2-6 Support functions (digital)

Table 2-7 Power supply pins

Table 2-8 Ground pins

Table 2-9 Do not connect (DNC) pins

Table 2-2 Pin descriptions – analog outputs and Rx processing

Pad #	Pad name and/or function	Pad name or alt function	Pad type [1]	Functional description
L4	EARO_M		AO	Earpiece amplifier output, differential minus
L3	EARO_P		AO	Earpiece amplifier output, differential plus
K1	HPH_LP		AO	Headphone left (plus) output
K2	HPH_RM		AO	Headphone right (minus) output
L2	HPH_REF		AI, AO	Capless headphone PA's ground reference
K6	LINE_OUT1		AO	Audio line output 1, single-ended
L9	LINE_OUT2		AO	Audio line output 2, single-ended
L6	LINE_OUT3		AO	Audio line output 3, single-ended
L8	LINE_OUT4		AO	Audio line output 4, single-ended
K5	LINE_OUT5		AO	Audio line output 5, single-ended

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-3 Pin descriptions – analog inputs and Tx processing

Pad #	Pad name and/or function	Pad name or alt function	Pad type [1]	Functional description
A9	MIC_IN1_P		AI	Microphone input 1, differential plus
A8	MIC_IN1_M		AI	Microphone input 1, differential minus
D11	MIC_IN2_P		AI	Microphone input 2, differential plus
D10	MIC_IN2_M		AI	Microphone input 2, differential minus
F11	MIC_IN3_P		AI	Microphone input 3, differential plus
F10	MIC_IN3_M		AI	Microphone input 3, differential minus
B11	MIC_IN4_P		AI	Microphone input 4, differential plus
C10	MIC_IN4_M		AI	Microphone input 4, differential minus
J11	MIC_IN5_P		AI	Microphone input 5 and AUX PGA left input, differential plus
K11	MIC_IN5_M		AI	Microphone input 5 and AUX PGA left input, differential minus
K8	MIC_IN6_P		AI	Microphone input 6 and AUX PGA right input, differential plus
K7	MIC_IN6_M		AI	Microphone input 6 and AUX PGA right input, differential minus
K9	MBHC_IN	MIC_IN7	AI	Multibutton headset control input Microphone input 7, single-ended

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-4 Pin descriptions – digital data I/Os

Pad #	Pad name and/or function	Pad name or alt function	Pad type [1]	Functional description
SLIMbus bidirectional multiplexed audio				
B1	SB_DATA	RX_I2S_SD2	B B	Bidirectional (Rx/Tx) SLIMbus data I2C serial data
A2	SB_CK	RX_I2S_SD1	B B	Bidirectional (Rx/Tx) SLIMbus clock I2C serial clock
I²S bus – Rx direction				
B1	RX_I2S_SD2	SB_DATA	DI B	I²S serial data line 2, Rx direction Bidirectional (Rx/Tx) SLIMbus data
A2	RX_I2S_SD1	SB_CK	DI B	I²S serial data line 1, Rx direction Bidirectional (Rx/Tx) SLIMbus clock
E2	RX_I2S_SCK		B	I²S bit clock, Rx direction
C1	RX_I2S_WS		B	I²S word select, Rx direction
I²S bus – Tx direction				
D7	TX_I2S_SD2	DMIC_CK2	DO DO	I²S serial data line 2, Tx direction Clock for digital microphones 5 and 6
A4	TX_I2S_SD1	DMIC_D2	DO DI	I²S serial data line 1, Tx direction Data for digital microphones 5 and 6
B5	TX_I2S_SCK		B	I²S bit clock, Tx direction
D3	TX_I2S_WS		B	I²S word select, Tx direction
Digital microphone (DMIC) interfaces				
B3	DMIC_D0		DI	Data for digital microphones 1 and 2
E6	DMIC_CK0		DO	Clock for digital microphones 1 and 2
F5	DMIC_D1		DI	Data for digital microphones 3 and 4
C4	DMIC_CK1		DO	Clock for digital microphones 3 and 4
A4	DMIC_D2	TX_I2S_SD1	DI DO	Data for digital microphones 5 and 6 I²S serial data line 2, Tx direction
D7	DMIC_CK2	TX_I2S_SD2	DO	Clock for digital microphones 5 and 6

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-5 Pin descriptions – support functions (analog)

Pad #	Pad name and/or function	Pad name or alt function	Pad type [1]	Functional description
Charge pump				
F2	CP_VPOS		AO	Charge pump voltage plus output
J2	CP_VNEG		AO	Charge pump voltage minus output
H2	CP_C1_P		AI, AO	Charge pump transfer capacitor, plus side
H1	CP_C1_M		AI, AO	Charge pump transfer capacitor, minus side
Low dropout (LDO) linear regulator				
H7	LDOL_CAP	VDD_TXADC	AO P	LDO low output load capacitor Power for Tx ADC circuits
H11	LDOH_CAP		AO	Internal circuitry LDO high output load capacitor
Microphone bias voltages and decoupling				
A10	MIC_BIAS1		AO	Microphone bias output voltage 1
D9	MIC_BIAS2		AO	Microphone bias output voltage 2
F9	MIC_BIAS3		AO	Microphone bias output voltage 3
H9	MIC_BIAS4		AO	Microphone bias output voltage 4
B8	MICB_CFILT1		AO	Microphone bias circuit compensation capacitor 1
G10	MICB_CFILT2		AO	Microphone bias circuit compensation capacitor 2
H10	MICB_CFILT3		AO	Microphone bias circuit compensation capacitor 3
Bandgap voltage reference (V_{REF}) decoupling				
L10	CCOMP		AO	Bandgap reference circuit compensation capacitor

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-6 Pin descriptions – support functions (digital)

Pad #	Pad name and/or function	Pad name or alt function	Pad type [1]	Functional description
Clock circuits				
C8	MCLK		AI	Master clock input
Inter-integrated circuit (I^2C) port				
B6	I2C_SDA		B	I2C serial data
D1	I2C_SCL		B	I2C serial clock
Discrete status and control signals				
F3	MODE0		DI	Digital interface mode selection (SLIMbus or I^2S) pin 1
G4	MODE1		DI	Digital interface mode selection (SLIMbus or I^2S) pin 2
H5	RESET_N		DI	WCD9311 IC-level reset
B7	INTR_OUT		DO	Interrupt output (active high)

1. Refer to Table 2-1 for parameter and acronym definitions.

Table 2-7 Pin descriptions – Power supply pins

Pad #	Pad name	Functional description
H7	VDD_TXADC	Power for Tx ADC circuits
F1	VDD_CP	Power for charge pump analog circuits
D5	VDD_DIG	Power for digital circuits
C6	VDD_IO	Power for digital I/O pads
G8	VDD_VBAT	Power for the LDO and microphone bias circuits
G6	VDDA_RX	Power for Rx-path analog circuits
E10	VDDA_TX	Power for Tx-path analog circuits

Table 2-8 Pin descriptions – Ground pins

Pad #	Pad name	Functional description
G2, H3, J4, E4, J8, A6, E8, F7	GND	Ground
J6	GND_CCOMP	Ground for V_{REF} compensator cap; connect to CCOMP capacitor and PCB ground

Table 2-9 Pin descriptions – Do not connect (DNC) pins

Pad #	Pad name	Functional description
A1, A11, A3, B10, B2, B4, B9, C2, D2, J10, K10, K3, K4, L1, L11	DNC	Do not connect

3 Electrical Specifications

3.1 Absolute maximum ratings

Operating the WCD9311 device under conditions beyond its absolute maximum ratings (Table 3-1) may damage the device. Absolute maximum ratings are limiting values to be considered individually when all other parameters are within their specified operating ranges. Functional operation and specification compliance under any absolute maximum condition, or after exposure to any of these conditions, is not guaranteed or implied. Exposure may affect device reliability.

Table 3-1 Absolute maximum ratings

Parameter	Description	Min	Max	Units
DC power supplies				
VDD_VBAT	Battery input voltage	-0.3	4.7	V
VDD_CP	Charge pump supply	-0.3	2.3	V
VDDA_TX	Tx path power	-0.3	2.3	V
VDDA_RX	Rx path power	-0.3	2.3	V
VDD_TXADC	General analog circuits	-0.3	1.44	V
VDD_IO	Digital I/Os	-0.3	2	V
VDD_DIG	Digital core circuits	-0.3	1.44	V
Signal pins				
V_{in_dig}	Any digital input nonpower	-0.3	2	V
V_{out_dig}	Any digital output nonpower	-0.3	1.9	V
V_{in_ana}	Any analog input nonpower	-0.3	2.9	V
V_{out_ana}	Any analog output nonpower	-0.3	2.9	V
Thermal conditions – see Section 4.4.				
ESD protection – see Chapter 7.				

3.2 Recommended operating conditions

Operating conditions include parameters that are under the control of the user: power-supply voltage and ambient temperature (Table 3-2). The WCD9311 device meets all performance specifications listed in Section 3.3 through Section 3.10, when used within the recommended operating conditions, unless otherwise noted in those sections (provided the absolute maximum ratings have never been exceeded – see Section 3.1).

Table 3-2 Recommended operating conditions

Parameter	Description	Min	Typ	Max	Units
Power supplies					
VDD_VBAT	Battery input voltage	2.50	3.80	4.50	V
VDD_CP	Charge pump supply	1.70	2.20	2.30	V
VDDA_TX	Tx path power	1.70	2.20	2.30	V
VDDA_RX	Rx path power	1.70	2.20	2.30	V
VDD_TXADC	Tx ADC analog circuit power	1.10	1.20	1.35	V
VDD_IO	Digital I/Os	1.70	1.80	1.90	V
VDD_DIG	Digital core circuits	1.14	1.20	1.35	V
LDOH	Linear dropout high output voltage				
LDOH = 2.05 V [1]		2.00	2.05	2.10	V
LDOH = 2.35 V [2]		2.30	2.35	2.40	V
LDOH = 2.75 V [2]		2.70	2.75	2.80	V
LDOL	Linear dropout low output voltage [3]	1.25	1.3	1.35	V
Thermal condition					
Tc	Operating temperature (case)	-30	–	85	ºC

1. Input to LDOH is 2.2 V and could be from the PM8921 device SMPS.
2. Input to LDOH is VPH_PWR (default).
3. Input to LDOL is 1.8 V and could be from the PM8921 device SMPS. (LDOL is not used by default.)

3.3 DC power characteristics

3.3.1 Peak current

Table 3-3 Power supply peak current

Parameter	Comments	Min	Typ	Max	Units
VDD_VBATT		–	–	20	mA
VDD_CP		–	–	500	mA
VDDA_TX		–	–	20	mA
VDDA_RX		–	–	20	mA
VDD_TXADC		–	–	5	mA
VDD_IO		–	–	5	mA
VDD_DIG		–	–	5	mA
LDOH		–	–	20	mA
LDOL		–	–	5	mA

3.3.2 Power consumption for typical use cases

Table 3-4 Power consumption for typical use cases

Scenario	Test conditions [1]	Typical current (µA)						
		VBAT (3.8 V)	VDD_CP (1.8 V)	VDDA_RX and VDDA_TX (1.8 V)	VDD_A (1.2 V)	VDD_DIG_IO (1.8 V)	VDD_DIG (1.2 V)	Total power [2] (mW)
Reset	WCD in reset (reset pin held high), MCLK off	1.80	0.05	0.16	0.45	0.04	2.86	0.01
Standby (idle)	WCD taken out of reset, MCLK off	1.80	0.05	0.16	0.44	0.05	2.86	0.01
Stereo playback to HPH	48 kHz, 16 bits, 16 Ω load, quiescent							
	48 kHz, 24 bits, 16 Ω load quiescent	1.40	812.40	726.60	6.80	24.40	988.60	4.01
	48 kHz, 16 bits, 16 Ω load. 0.1 mW delivered to load							
	48 kHz, 24 bits, 16Ω load. 0.1 mW delivered to load	0.80	2810.60	744.60	6.80	29.80	1077.20	7.76
Stereo playback to stereo line output	48 kHz, 16 bits, 10 kΩ load							
	48 kHz, 24 bits, 10 kΩ load	4.00	4.00	1445.00	3.00	40.00	640.00	3.47
Stereo playback to mono-differential line output	48 kHz, 16 bits, 10 kΩ load							
	48 kHz, 24 bits, 10 kΩ load	20.00	3.00	1483.00	4.00	40.00	610.00	3.56
Device voice call	Analog mic, EAR PA 32 Ω, mono 8 kHz sample rate, 16 bits	258.00	645.00	741.00	162.00	110.00	1120.00	5.21
	Analog mic, EAR PA 32 Ω, mono 16 kHz sample rate, 16 bits	264.00	646.00	736.00	159.00	110.00	1120.00	5.22
	Stereo analog mics, EAR PA 32 Ω mono 8 kHz sample rate, 16 bits	258.00	644.00	920.00	325.00	110.00	1210.00	5.84
	Stereo digital mics, EAR PA 32 Ω mono 8 kHz sample rate, 16 bits	258.00	647.00	914.00	323.00	130.00	1210.00	5.86
	Digital mic (2.4 MHz), EAR PA 32 Ω, mono 8 kHz, 16 bits	268.00	647.00	470.00	3.00	170.00	930.00	4.45
	Digital mic (2.4 MHz), EAR PA 32Ω, mono 16 kHz, 16 bits	268.00	647.00	470.00	5.00	190.00	840.00	4.39

Table 3-4 Power consumption for typical use cases (cont.)

Scenario	Test conditions [1]	Typical current (µA)						
		VBAT (3.8 V)	VDD_CP (1.8 V)	VDDA_RX and VDDA_TX (1.8 V)	VDD_A (1.2 V)	VDD_DIG_IO (1.8 V)	VDD_DIG (1.2 V)	Total power [2] (mW)
Headset voice call	Mono analog mic, stereo HPH 16 Ω 8 kHz, 16 bits	568.00	783.00	981.00	159.00	10.00	1060.00	6.81
	Mono digital mic (2.4 MHz), stereo HPH 16 Ω 8 kHz sample rate, 16 bits	269.00	782.00	731.00	4.00	180.00	1040.00	5.32
Speaker phone mode	Mono analog mic, mono-differential line output 8 kHz, 16 bits	218.00	4.00	1695.00	162.00	30.00	810.00	5.11
Stereo FM playback	Stereo line input to AUX_PGA, stereo HPH 16Ω 48 kHz sample rate, 16 bits	4.00	2176.00	633.00	3.00	50.00	900.00	6.25
	Stereo line input to AUX_PGA, stereo line output 10 kΩ 48 kHz sample rate, 16 bits	4.00	3.00	1140.00	5.00	50.00	50.00	2.23
Stereo recording	Dual analog mics capless, 16 bits, 48 kHz sample rate	20.00	3.00	523.00	324.00	70.00	720.00	2.40

1. Unless otherwise specified, all measurements are in quiescent mode.
2. Power values show what would be consumed by the WCD9311 device only.

3.4 Powerup sequence

This information will be included in future revisions of this document.

3.5 Digital logic characteristics

Table 3-5 Digital I/O characteristics

Parameter		Comments [1]	Min	Typ	Max	Units
V_{IH}	High-level input voltage		0.65 · V_{DDX}	–	1.1 · V_{DDX}	V
V_{IL}	Low-level input voltage		0.10 · V_{DDX}	–	0.35 · V_{DDX}	V
V_{OH}	High-level output voltage		0.90 · V_{DDX}	–	V_{DDX}	V
V_{OL}	Low-level output voltage		0	–	0.10 · V_{DDX}	V
C_{IN}	Digital input capacitance		–	–	5	pF

1. V_{DDX} is the supply voltage associated with the digital I/O pin being tested (connected to the VDD_IO pin).

3.6 Audio inputs and Tx processing

Unless otherwise stated, all Tx performance parameters are measured at the 48 kHz sampling rate.

3.6.1 Analog input through digital serial interface

Performance of the following Tx path is specified in Table 3-6: any analog input – pre-amp – ADC – digital serial interface.

Table 3-6 Analog input through digital serial interface performance

Parameter	Comments	Min	Typ	Max	Units
Microphone amplifier gain = 0 dB (minimum gain)					
Input referred noise	Differential or single-ended; A-weighted				
Capless mode	VDDA_TX = 1.8 V or 2.2 V	–	9.2	11.5	µVrms
Cap-coupled mode	VDDA_TX = 1.8 V or 2.2 V	–	9.2	11.5	µVrms
SNR	Capless or cap-coupled mode				
Differential input	VDDA_TX = 2.2 V	99.0	102.0	–	dB
	VDDA_TX = 1.8 V	93.0	96.0	–	dB
Single-ended input	VDDA_TX = 2.2 V	93.0	96.0	–	dB
	VDDA_TX = 1.8 V	90.0	93.0	–	dB
THD + N ratio	Capless or cap-coupled mode; VDDA_TX = 1.8 V or 2.2 V; f = 1.02 kHz; band-limited at 200 Hz to 20 kHz				
Differential input	Input level = -1 dBV	86.0	91.0	–	dB
Differential or SE input	Input level = -60 dBV	34.0	41.0	–	dB

Table 3-6 Analog input through digital serial interface performance (cont.)

Parameter	Comments	Min	Typ	Max	Units
Microphone amplifier gain = 18 dB (maximum gain)					
Input referred Noise	Differential or single-ended; A-weighted				
Capless mode	VDDA_TX = 1.8 V or 2.2 V	–	4.4	5.6	µVrms
Cap-coupled mode	VDDA_TX = 1.8 V or 2.2 V	–	3.7	5.0	µVrms
SNR	Differential or single-ended input				
Capless mode	VDDA_TX = 1.8 V or 2.2 V	87.0	89.0	–	dB
Cap-coupled mode	VDDA_TX = 1.8 V or 2.2 V	88.0	90.0	–	dB
THD + N ratio	Capless or cap-coupled mode; VDDA_TX = 1.8 V or 2.2 V; f = 1.02 kHz; band-limited at 200 Hz to 20 kHz				
Differential input	Input level = -19 dBV	70.0	78.0	–	dB
Differential or SE input	Input level = -60 dBV	23.0	29.0	–	dB
Other characteristics					
Full-scale input voltage	Differential 1 kHz input. Input signal level required to get 0 dBFS digital output; VDDA_TX = 1.8 or 2.2 V capless or cap-coupled mode	-0.5	0	0.5	dBv
Absolute gain error	-20 dBv input level, 1.02 kHz, VDDA_TX = 1.8 or 2.2 V	-0.5	–	0.5	dB
Power supply rejection	1.8 or 2.2 V analog; 100 mVpp square wave imposed on power supply; analog input = 0 Vrms				
0 kHz < f < 1 kHz	Terminated with 2 kΩ; keep bypass caps on the pwr pin and measure 100 mV ripple at the pwr pin	51.0	56.0	–	dB
1 kHz < f < 5 kHz		51.0	56.0	–	dB
5 kHz < f < 2 0 kH		51.0	56.0	–	dB
Input impedance	All gain modes				
Cap-coupled, differential		16.0	20.0	24.0	kΩ
Cap-coupled, single-ended		8.0	10.0	12.0	kΩ
Capless		1.0	–	–	MΩ
Input disabled		3.0	–	–	MΩ
Input capacitance					
Analog pin		–	–	15	pF
Digital pin		–	–	5	pF
Capless input mode		–	–	15	pF
Rx to Tx cross-talk attenuation	Tx path measurement with -5 dBFS Rx path signal. f = 1 kHz	90.0	100.0	–	dB
Interchannel isolation	20 < f < 20 kHz; IN_1 terminated with 1 kΩ; IN_2 = -5 dBFS at 1 kHz. Measure digital output of terminated channel.	90.0	100.0	–	dB

Typical Tx path performance is shown in the following plots.

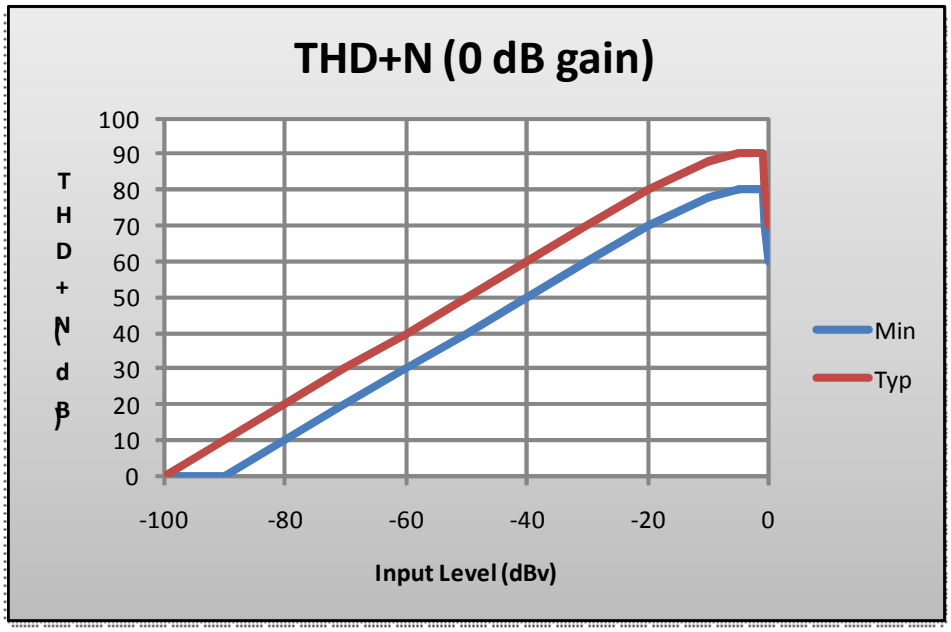


Figure 3-1 THD + N (0 dB gain)

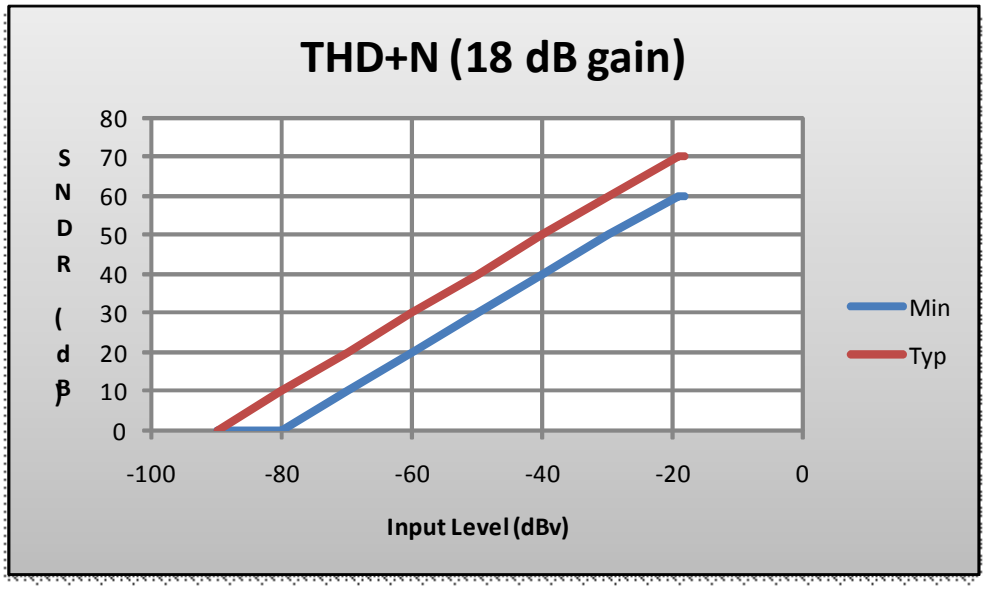


Figure 3-2 THD + N (18 dB gain)

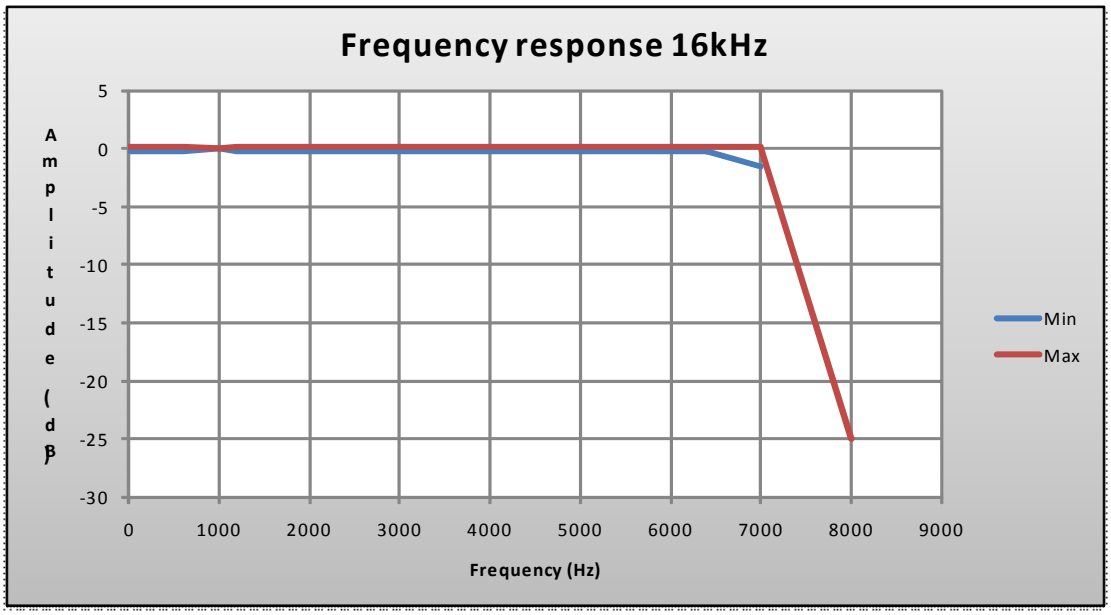


Figure 3-3 Frequency response (16 kHz)

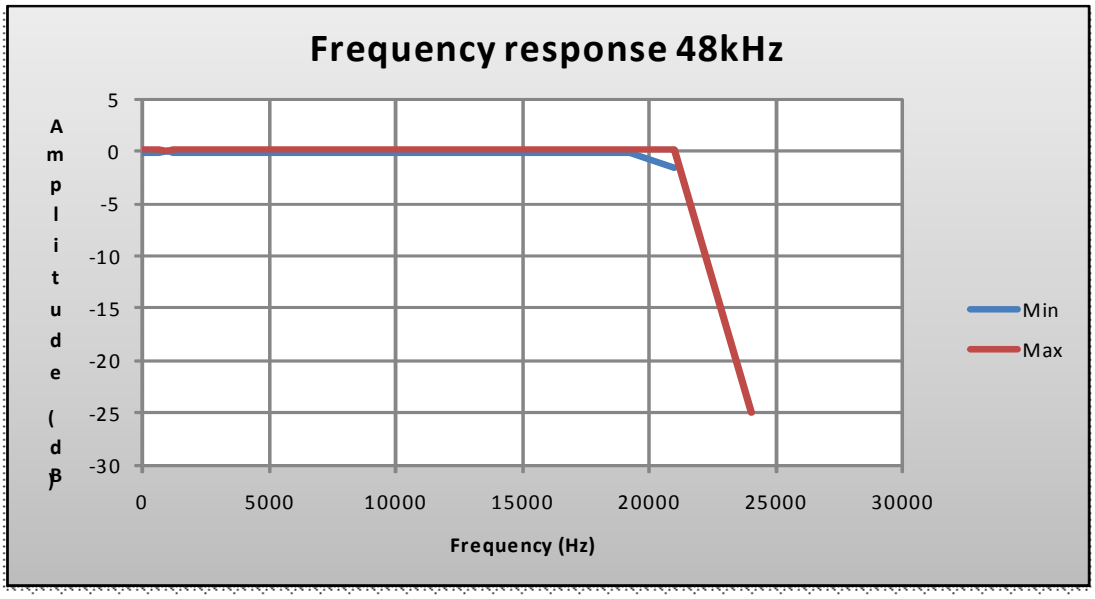


Figure 3-4 Frequency response (48 kHz)

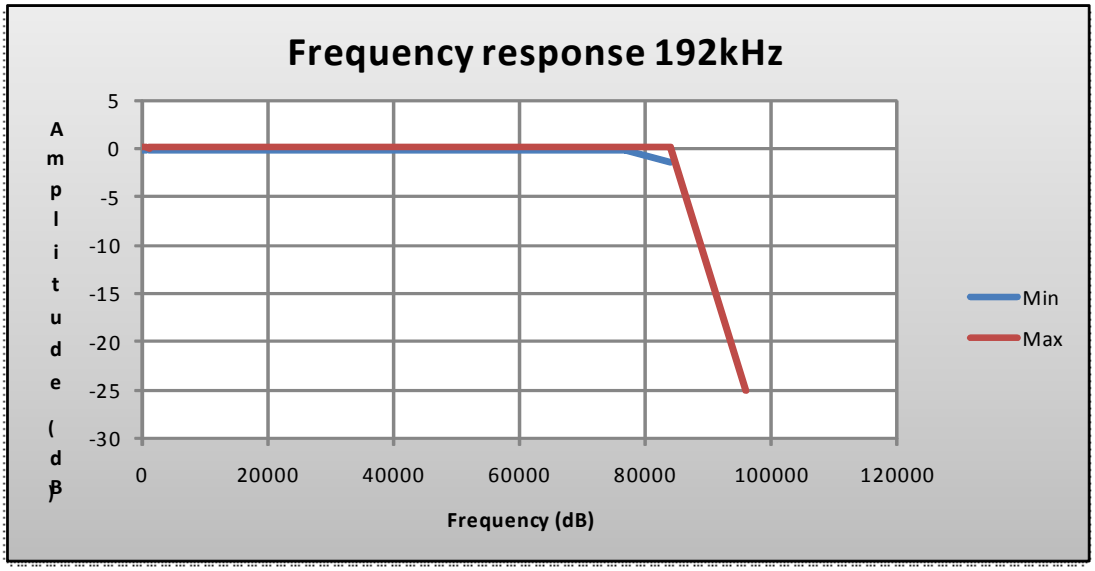


Figure 3-5 Frequency response (192 kHz)

3.6.2 DMIC input through digital serial interface

Performance of the following Tx path is specified in Table 3-7: any digital microphone input – digital serial interface.

Table 3-7 Digital microphone input through digital serial interface performance

Parameter	Comments	Min	Typ	Max	Units
16 kHz					
SNR	A-weighted	100.0	103.0	–	dB
THD + N	f = 1.02 kHz; band-limited to 200 Hz – 1/2 * Fs				
PCM out = -1 dBFS		84.0	85.0	–	dB
PCM out = -60 dBFS		40.0	41.0	–	dB
48 kHz					
SNR	PDM input	100.0	103.0	–	dB
THD + N	f = 1.02 kHz; band-limited to 200 Hz – 1/2 * Fs				
PCM out = -1 dBFS		94.0	95.0	–	dB
PCM out = -60 dBFS		42.0	43.0	–	dB
192 kHz					
SNR	PDM input, band-limited to 30 kHz – 1/2*Fs	39.0	40.0	–	dB
THD + N	f = 50 kHz; band-limited to 30 kHz – 1/2*Fs				
PCM out = -1 dBFS		35.0	36.0	–	dB
PCM out = -60 dBFS		-16.0	-15.0	–	dB
Other characteristics					
Full-scale input signal	1 bit PDM; 1 kHz				
Decimator gain = 6 dB		–	75/25	–	%
Decimator gain = 0 dB		–	100/0	–	%
Interchannel gain mismatch	1 kHz, -20 dBFS	–	0.10	0.20	dB
Clock rate	Decimated output rates: 8 kHz, 16 kHz, 32 kHz, and 48 kHz, 192 kHz				
MCLK = 9.6 MHz		–	2.400	–	MHz
MCLK = 12.288 MHz		–	2.048	–	MHz
MCLK = 24.576 MHz		–	3.072	–	MHz
Clock duty cycle	f = 1.024 MHz to 4.096 MHz	40/60	–	60/40	%
Input capacitance		–	1.0	5.0	pF
Board capacitance		–	10.0	50.0	pF

3.7 Audio outputs and Rx processing

Unless otherwise stated, all Rx performance parameters are measured at the 48 kHz sampling rate.

3.7.1 Digital serial interface through earpiece analog output

Performance of the following Rx path is specified in Table 3-8: digital serial input – mono DAC – mono EAR output.

Table 3-8 ^{Out} Serial interface through mono EAR output

Parameter	Comments	Min	Typ	Max	Units
EAR output; 8 kHz; 16 bits					
Receive noise	A-weighted				
6 dB gain (125 mW mode)		–	9.5	12.0	µVrms
2 dB gain (50 mW mode)		–	6.7	9.0	µVrms
SNR	Ratio of full-scale output to output noise level, 2 or 6 dB gain	102.0	105.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; 2 or 6 dB gain				
PCMI = -1 dBFS		68.0	72.0	–	dB
PCMI = -60 dBFS		32.0	38.0	–	dB
EAR output; 48 kHz; 16 bits					
Receive noise	A-weighted				
6 dB gain (125 mW mode)		–	9.5	12.0	µVrms
2 dB gain (50 mW mode)		–	6.7	9.0	µVrms
SNR	Ratio of full-scale output to output noise level, 2 or 6 dB gain	102.0	105.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; 2 or 6 dB gain				
PCMI = -1 dBFS		84.0	89.5	–	dB
PCMI = -60 dBFS		34.0	38.0	–	dB
EAR output; 48 or 192 kHz; 24 bits					
Receive noise	A-weighted				
6 dB gain (125 mW mode)		–	9.5	12.0	µVrms
2 dB gain (50 mW mode)		–	6.7	9.0	µVrms
SNR	Ratio of full-scale output to output noise level, 2 or 6 dB gain	102.0	105.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; 2 or 6 dB gain				
PCMI = -1 dBFS		83.0	89.0	–	dB
PCMI = -60 dBFS		41.0	47.0	–	dB

Table 3-8 Serial interface through mono EAR output (cont.)

Parameter	Comments	Min	Typ	Max	Units
Other characteristics					
Full-scale output voltage	PCMI = 0 dBFS, 1.02 kHz sine wave				
6 dB PA gain mode		5.5	6.0	6.5	dBv
2 dB PA gain mode		1.6	2.1	2.6	dBv
Absolute gain error	-20 dBFS input level, 1.02 kHz	-0.5	–	0.5	dB
Output DC offset	PCMI = -999 dBFs		1.0	3.0	mV
Output common mode voltage	PCMI = -999 dBFs	-0.05	0	0.05	V
Tx to Rx cross-talk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz	90.0	100.0	–	dB
Power supply rejection	100 mVpp squarewave imposed on power supply; digital input = -999 dBFS				
0 kHz < f < 1 kHz		80.0	85.0	–	dB
1 kHz < f < 5 kHz		70.0	80.0	–	dB
5 kHz < f < 20 kHz		70.0	75.0	–	dB
Disabled output impedance	Measured externally with amplifier disabled	1	–	–	MΩ
Output capacitance	Total capacitance between EAROP and EAROM, including PCB capacitance and EMI	–	–	500	pF
Turn on/off click and pop level	A-weighted; 10 kΩ; 1 µF; 50 ms	–	-65.0	-58.0	dBVpp

Typical EAR path THD + N performance and a 16 kHz frequency response curve is shown in the following plots.

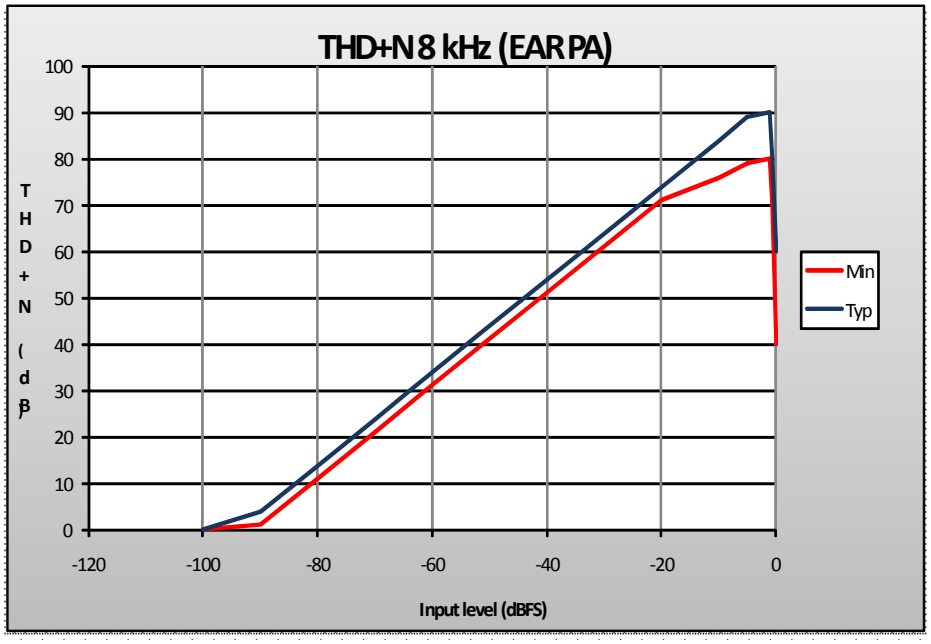


Figure 3-6 THD + N 8 kHz (EAR PA)

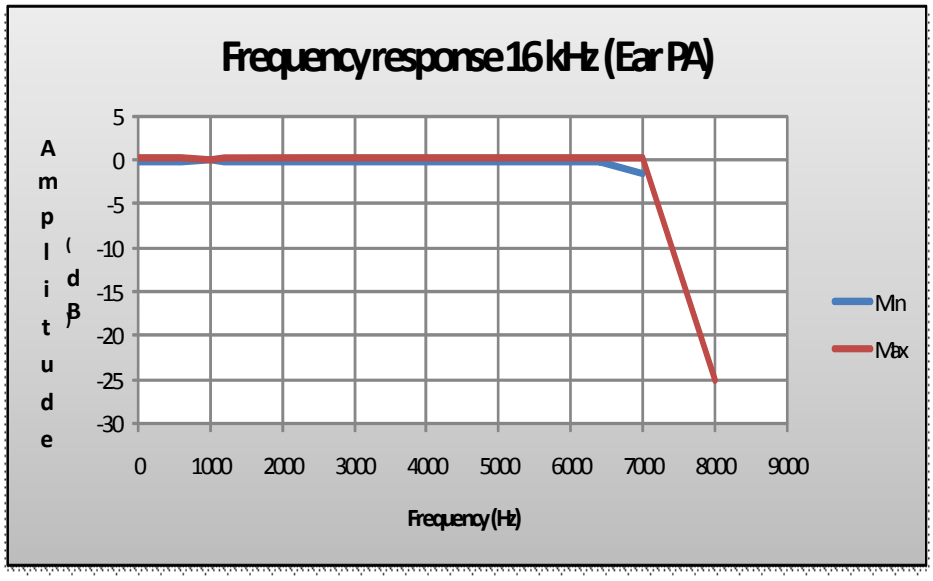


Figure 3-7 Frequency response 16 kHz (EAR PA)

3.7.2 Digital serial interface through stereo HPH output

Performance of the following Rx path is specified in Table 3-9: digital serial input – stereo DAC – stereo HPH output.

Table 3-9 Serial interface through stereo HPH output

Parameter	Comments	Min	Typ	Max	Units
HPH; 8 kHz; 16 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	4.5	6.0	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.6	7.1	µVrms
SNR	Ratio of full-scale output to output noise level				
VDDA_RX = 1.8 V		101.0	102.5	–	dB
VDDA_RX = 2.2 V		104.0	105.5	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; VDDA_RX = 1.8 V or 2.2 V				
PCMI = -1 dBFS		68.0	72.0	–	dB
PCMI = -60 dBFS		36.0	38.0	–	dB
HPH; 48 kHz; 16bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	4.5	6.0	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.6	7.1	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.2	3.5	µVrms
SNR	Ratio of full-scale output to output noise level				
VDDA = 1.8 V		101.0	102.5	–	dB
VDDA = 2.2 V		104.0	105.5	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; VDDA_RX = 1.8 V or 2.2 V				
PCMI = -1 dBFS		84.0	89.0	–	dB
PCMI = -60 dBFS		38.0	40.0	–	dB
HPH; 48 or 192 kHz; 24 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	4.5	6.0	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.6	7.1	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.2	3.5	µVrms
SNR	Ratio of full-scale output to output noise level; A-weighted				
VDDA = 1.8 V, no DRE		101.0	102.5	–	dB
VDDA = 2.2 V, no DRE		104.4	105.5	–	dB
VDDA_RX = 1.8 V, with DRE		106.0	108.0	–	dB
VDDA_RX = 2.2 V, with DRE		109.0	111.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz;				
PCMI = -1 dBFS	VDDA_RX = 1.8 V	84.0	89.0	–	dB
PCMI = -60 dBFS	VDDA_RX = 1.8, A-weighted	38.0	44.0	–	dB

Table 3-9 Serial interface through stereo HPH output (cont.)

Parameter	Comments	Min	Typ	Max	Units
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 0 dB FS; 16 Ω load				
VDDA_RX = 1.8 V		0.65	0.69	0.73	Vrms
VDDA_RX = 2.2 V		0.91	0.97	1.03	Vrms
Output power	f = 1.02 kHz, 0 dB FS				
VDDA_RX = 1.8 V	16 Ω load	26.4	29.7	33.3	mW
	32 Ω load	25.8	29.4	33.1	mW
VDDA_RX = 2.2 V	16 Ω load	51.7	58.8	66.3	mW
	32 Ω load	25.8	29.4	33.1	mW
Output load					
16 Ω nominal		13.0	16.0	50000	Ω
32 Ω nominal		26.0	32.0	50000	Ω
Tx to Rx cross-talk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz	90.0	100.0	–	dB
Inter-channel isolation	20 < f < 20 kHz; measured channel output = -999 dBFS; second DAC channel output = -5 dBFS	90.0	100.0	–	dB
Inter-channel gain error	Delta between left and right channels, input = 1 kHz at -20 dBFS	–	0	0.3	dB
Interchannel phase error	Delta between left and right channels. Input = 1 kHz at -20 dBFS	–	0	0.5	deg
Power supply rejection	100 mVpp squarewave imposed on power supply; digital input = -999 dBFS				
0 kHz < f < 1 kHz		80.0	90.0	–	dB
1 kHz < f < 5 kHz		70.0	80.0	–	dB
5 kHz < f < 20 kHz		60.0	70.0	–	dB
Disabled output impedance	Measured externally, with amplifier disabled	1.0	–	–	MΩ
Output capacitance	Total capacitance on HPH output singled ended, including PCB capacitance and EMI	–	–	1000	pF
Output DC offset		-0.81	0	0.81	mV
Turn on click and pop level	A-weighted	–	-86.0	-80.0	dBVpp
Turn off click and pop level	A-weighted	–	-75.0	-70.0	dBVpp
Turn on/off click and pop level	A-weighted, with DRE	–	-90.0	-80.0	dBVpp

Typical HPH path THD + N performance and a 48 kHz frequency response curve is shown in the following plots.

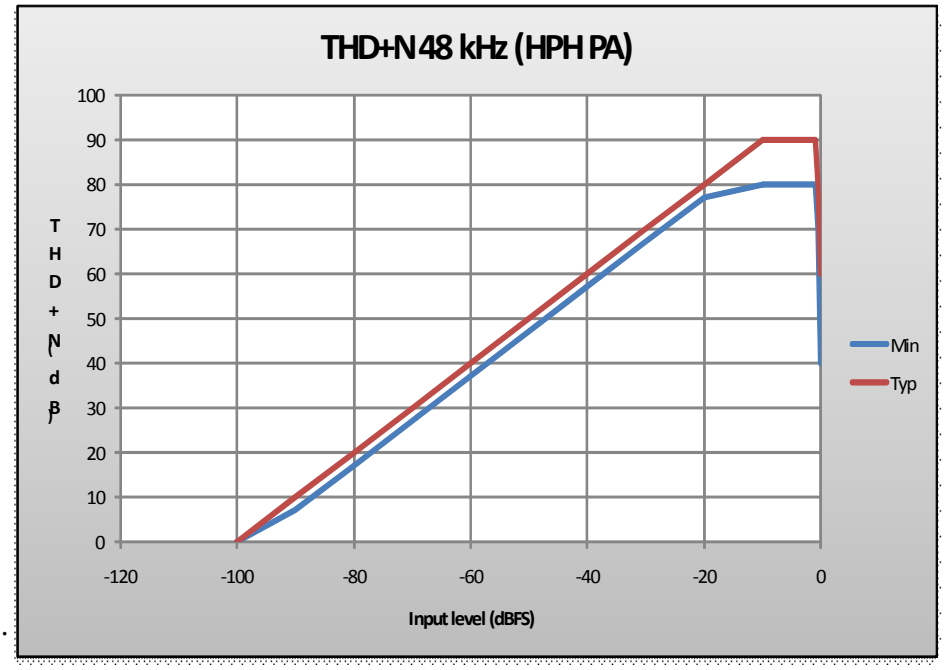


Figure 3-8 THD + N 48 kHz (HPH PA)

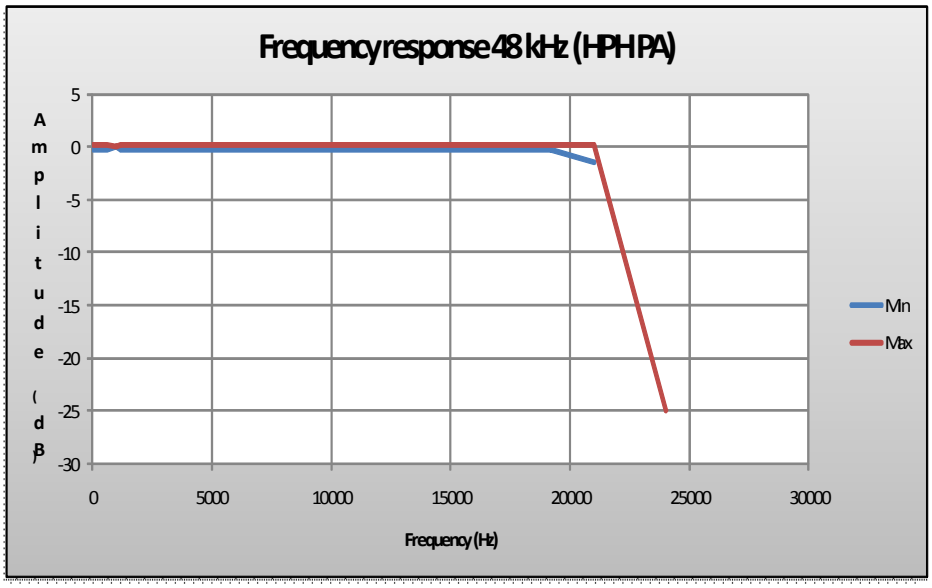


Figure 3-9 Frequency response 48 kHz (HPH PA)

3.7.3 Digital serial interface through stereo line output

Performance of the following Rx path is specified in Table 3-10: digital serial input – stereo DAC – stereo LINE output.

Table 3-10 Serial interface through stereo LINE output

Parameter	Comments	Min	Typ	Max	Units
Line output; 8 kHz; 16 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	3.6	5.0	µVrms
VDDA_RX = 2.2 V, no DRE		–	4	5.5	µVrms
SNR	Ratio of full-scale output to output noise level				
VDDA_RX = 1.8 V, no DRE		102.0	104.5	–	dB
VDDA_RX = 2.2 V, no DRE		102.0	104.5	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; VDDA_RX = 1.8 V or 2.2 V, A-weighted				
PCMI = -1 dBFS		68.0	72.0	–	dB
PCMI = -60 dBFS		33.0	36.0	–	dB
Line output; 48 kHz 16 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	3.6	5.0	µVrms
VDDA_RX = 2.2 V, no DRE		–	4.0	5.4	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.3	3.5	µVrms
SNR	Ratio of full-scale output to output noise level; A-weighted				
VDDA_RX = 1.8 V, no DRE		99.0	101.5	–	dB
VDDA_RX = 2.2 V, no DRE		101.5	103.0	–	dB
VDDA_RX = 2.2 V, with DRE		104.5	106.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; VDDA_RX = 1.8 V or 2.2 V				
PCMI = -1 dBFS		82.0	88.0	–	dB
PCMI = -60 dBFS		34.0	39.0	–	dB
Line output; 48 or 192 kHz; 24 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	3.6	5.0	µVrms
VDDA_RX = 2.2 V, no DRE		–	4.0	5.4	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.3	3.5	µVrms
SNR	Ratio of full-scale output to output noise level; A-weighted				
VDDA = 1.8 V, no DRE		99.0	101.5	–	dB
VDDA = 2.2 V, no DRE		101.5	103.0	–	dB
VDDA_RX = 2.2 V, with DRE		104.5	106.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz;				
PCMI = -1 dBFS	VDDA_RX = 1.8 V or 2.2 V	82.0	90.0	–	dB
PCMI = -60 dBFS	VDDA_RX = 1.8, A-weighted	37.0	43.0	–	dB

Table 3-10 Serial interface through stereo LINE output (cont.)

Parameter	Comments	Min	Typ	Max	Units
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 0 dB FS; 600 Ω load				
VDDA_RX = 1.8 V		0.47	0.50	0.53	Vrms
VDDA_RX = 2.2 V		0.56	0.60	0.63	Vrms
Output common mode voltage	PCMI = -999 dBFs				
VDDA_RX = 1.8 V		0.80	0.85	0.90	V
VDDA_RX = 2.2 V		1.00	1.05	1.10	V
Output load	Single ended	–	600	1 M	Ω
Tx to Rx cross-talk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz	90.0	100.0	–	dB
Inter-channel isolation	20 < f < 20 kHz; measured channel output = -999 dBFS; AUXPGA or second DAC channel output = -5 dBFS	90.0	100.0	–	dB
Power supply rejection	100 mVpp squarewave imposed on power supply; digital input = -999 dBFS; VDDA_RX = 2.2 V or 1.8 V analog				
0 kHz < f < 1 kHz		80.0	85.0	–	dB
1 kHz < f < 5 kHz		70.0	80.0	–	dB
5 kHz < f < 20 kHz		70.0	75.0	–	dB
Output impedance					
PA disabled	Measured externally, with amplifier disabled	1	–	–	MΩ
PA enabled	20 to 20 kHz bandwidth	–	–	10.0	Ω
Output capacitance	Total capacitance on LINE output singled ended, including PCB capacitance and EMI	–	–	1000	pF
Turn on click and pop level	A-weighted; 10 kΩ ohms; 1 µF; 50 ms	–	-56.0	-55.0	dBVpp
Turn off click and pop level	A-weighted; 10 kΩ ohms; 1 µF; 50 ms	–	-61.0	-55.0	dBVpp

3.7.4 Digital serial interface through mono-differential line outputs

Performance of the following Rx path is specified in Table 3-11: digital serial input – mono DAC – mono-differential LINE outputs.

Table 3-11 Serial interface through mono LINE outputs

Parameter	Comments	Min	Typ	Max	Units
Line output; 8 kHz 16 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	5.0	6.5	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.4	7.1	µVrms
SNR	Ratio of full-scale output to output noise level				
VDDA_RX = 1.8 V, no DRE		103.0	106.0	–	dB
VDDA_RX = 2.2 V, no DRE		104.5	107.0	–	dB
VDDA_RX = 2.2 V, with DRE		105.0	108.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; VDDA_RX = 1.8 V or 2.2 V, A-weighted				
PCMI = -1 dBFS		68.0	72.0	–	dB
PCMI = -60 dBFS		36.0	39.0	–	dB
Line output; 48 kHz 16 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	5.0	6.5	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.4	7.1	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.3	3.5	µVrms
SNR	Ratio of full-scale output to output noise level; A-weighted				
VDDA_RX = 1.8 V, no DRE		103.0	106.0	–	dB
VDDA_RX = 2.2 V, no DRE		104.5	107.0	–	dB
VDDA_RX = 2.2 V, with DRE		105.0	108.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz; VDDA_RX = 1.8 V or 2.2 V				
PCMI = -1 dBFS		91.0	97.0	–	dB
PCMI = -60 dBFS		33.0	39.0	–	dB
Line output; 48 kHz; 24 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	5.0	6.5	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.4	7.1	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.3	3.5	µVrms
SNR	Ratio of full-scale output to output noise level; A-weighted				
VDDA_RX = 1.8 V, no DRE		103.0	106.0	–	dB
VDDA_RX = 2.2 V, no DRE		104.5	107.0	–	dB
VDDA_RX = 2.2 V, with DRE		105.0	108.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz;				
PCMI = -1 dBFS	VDDA_RX = 1.8 V or 2.2 V	91.0	97.0	–	dB
PCMI = -60 dBFS	VDDA_RX = 1.8, A-weighted	33.0	39.0	–	dB

Table 3-11 Serial interface through mono LINE outputs (cont.)

Parameter	Comments	Min	Typ	Max	Units
Line output; 192 kHz; 24 bits					
Receive noise	A-weighted; input = -999 dBFS				
VDDA_RX = 1.8 V, no DRE		–	5.0	6.5	µVrms
VDDA_RX = 2.2 V, no DRE		–	5.4	7.1	µVrms
VDDA_RX = 1.8 V or 2.2 V, DRE enabled		–	2.3	3.5	µVrms
SNR	Ratio of full-scale output to output noise level; A-weighted				
VDDA_RX = 1.8 V, no DRE		103.0	106.0	–	dB
VDDA_RX = 2.2 V, no DRE		104.5	107.0	–	dB
VDDA_RX = 2.2 V, with DRE		105.0	109.0	–	dB
THD + N	Band-limited from 200 Hz to 20 kHz;				
PCMI = -1 dBFS	VDDA_RX = 1.8 V or 2.2 V	80.0	90.0	–	dB
PCMI = -60 dBFS	VDDA_RX = 1.8 V	35.0	38.0	–	dB
PCMI = -60 dBFS	VDDA_RX = 2.2 V, A-weighted	40.0	43.0	–	dB
Other characteristics					
Full-scale output voltage	f = 1.02 kHz, 0 dB FS; 600 Ω load				
VDDA_RX = 1.8 V		0.94	1.00	1.06	Vrms
VDDA_RX = 2.2 V		1.12	1.19	1.26	Vrms
Output common mode voltage	PCMI = -999 dBFs				
VDDA_RX = 1.8 V		0.80	0.85	0.90	V
VDDA_RX = 2.2 V		1.00	1.05	1.10	V
Output load	Single ended	–	600	1 M	Ω
Tx to Rx cross-talk attenuation	Rx path measurement with -5 dBFS Tx path signal. f = 1 kHz	90.0	100.0	–	dB
Inter-channel isolation	20 < f < 20 kHz; measured channel output = -999 dBFS; AUXPGA or second DAC channel output = -5 dBFS	90.0	100.0	–	dB
Power supply rejection	100 mVpp squarewave imposed on power supply; digital input = -999 dBFS; VDDA_RX = 1.8 V or 2.2 V				
0 kHz < f < 1 kHz		80.0	85.0	–	dB
1 kHz < f < 5 kHz		70.0	80.0	–	dB
5 kHz < f < 20 kHz		70.0	75.0	–	dB
Output impedance					
PA disabled	Measured externally with amplifier disabled	1.0	–	–	MΩ
PA enabled	PA active, 20 to 20 kHz bandwidth	–	–	10.0	Ω
Output capacitance	Total capacitance differentially across LINE output, including PCB capacitance and EMI	–	–	500	pF
Turn on/off click and pop level	A-weighted; 10 kΩ; 1 µF; 50 ms	–	-70.0	-55.0	dBVpp

Typical single-ended LINE path THD + N performance and a 192 kHz frequency response curve is shown in the following plots.

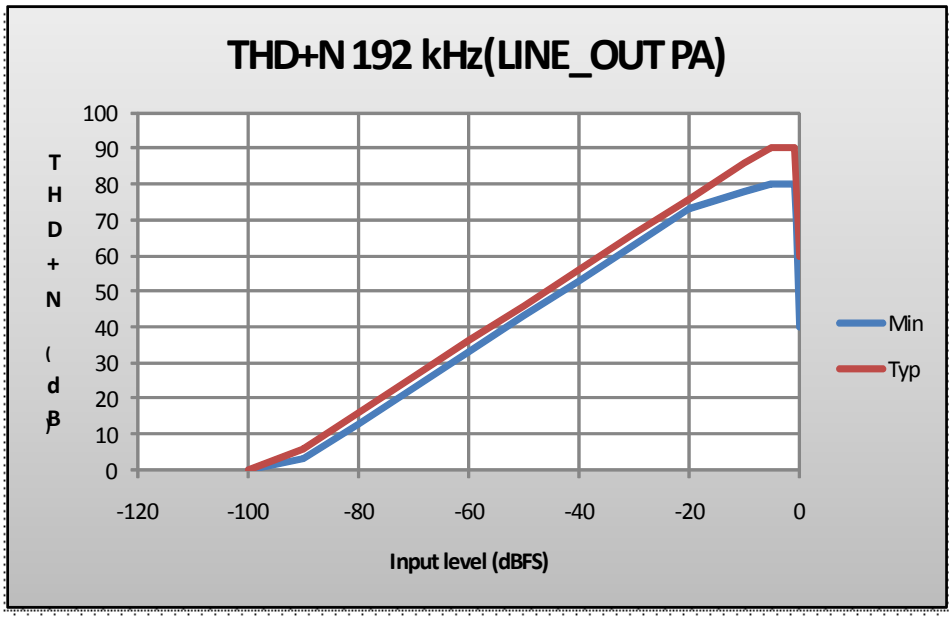


Figure 3-10 THD + N 192 kHz (LINE_OUT PA)

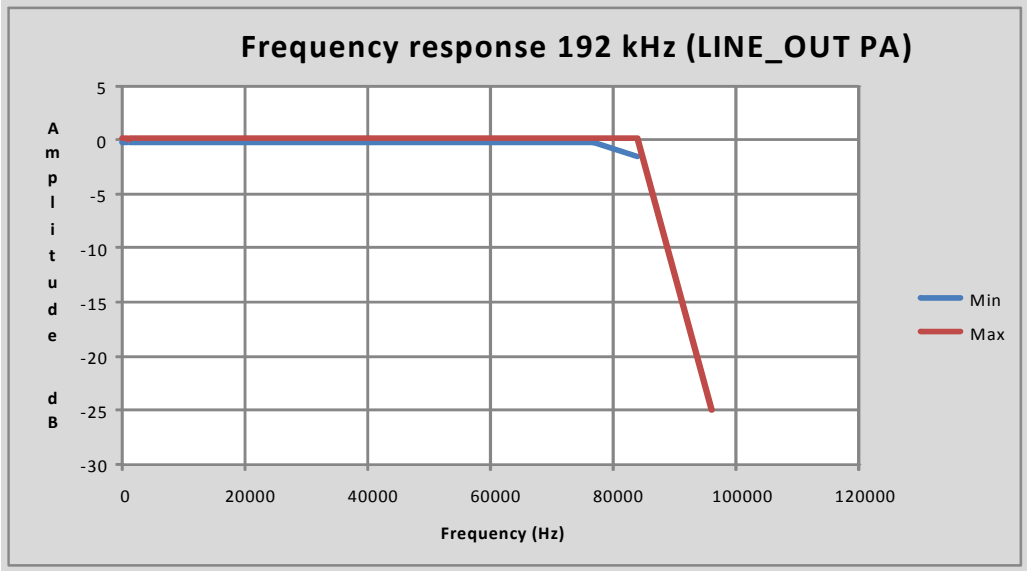


Figure 3-11 Frequency response 192 kHz (LINE_OUT PA)

3.8 Digital I/Os and digital processing

Digital logic characteristics are defined in Section 3.5. The supported industry standards are identified in the following subsections.

3.8.1 Serial low-power inter-chip media bus (SLIMbus)

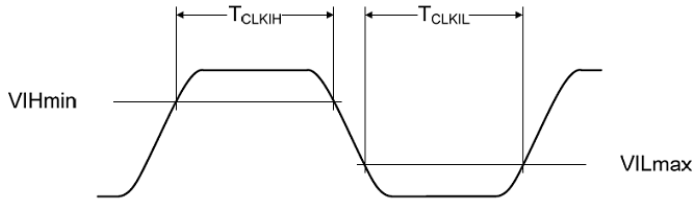


Figure 3-12 Received clock signal constraints

Table 3-12 Clock input timing requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_{CLKIH}	CLK input high time	I_{OL} = 1 mA	12	–	–	ns
V_{CLKIL}	CLK input low time	I_{OH} = 1 mA	12	–	–	ns
SR_{CLKI}	Clock input slew rate	20% < VI < 80%	0.02 * VDD	–	–	V/ns

Table 3-13 Data output timing characteristics

Symbol	Parameter	Condition	Min	Typ	Max	Units
SR_{DATA}	Data output slew rate	20% < VO < 80%	–	–	0.5 * VDD	V/ns
T_{DV}	Time for data output valid	I_{OH} = 1 mA	–	–	–	ns

Table 3-14 Data input timing requirements

Symbol	Parameter	Condition	Min	Typ	Max	Units
T_H	Data input hold time		2	–	–	ns
T_{SETUP}	Data input setup time		12	–	–	ns

3.8.2 Inter-IC sound (I2S)

Table 3-15 Supported I2S standards and exceptions

Applicable standards	Feature exceptions	WCD9311 variations
Phillips I2S Bus Specifications revised June 5, 1996	No external controller support	None

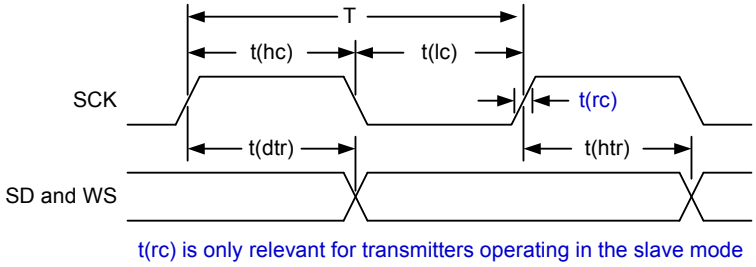


Figure 3-13 I2S transmitter timing diagram

Table 3-16 Master transmitter with data rate of 16 MHz

Symbol	Parameter	Comments	Min	Typ	Max	Units
T	Clock period	12S requirement: min T = 62.5	-	62.5	-	ns
t(hc)	Clock high	12S requirement: min > 0.35 T	-	-	-	ns
t(lc)	Clock low	12S requirement: min > 0.35 T	-	-	-	ns
t(dtr)	Delay	12S requirement: min < 0.8 T	-	-	15.6	ns
t(htr)	Hold time	12S requirement: min > 0	3.2	-	-	ns

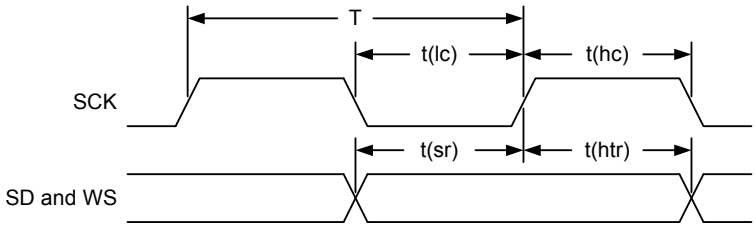


Figure 3-14 I2S receiver timing diagram

Table 3-17 Slave receiver with data rate of 16 MHz

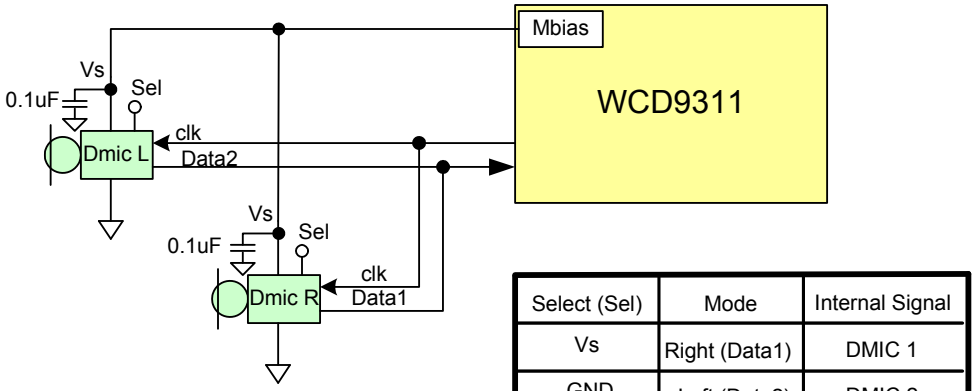
Symbol	Parameter	Comments	Min	Typ	Max	Units
T	Clock period	12S requirement: min T = 62.5	-	62.5	-	ns
t(hc)	Clock high	12S requirement: min < 0.35 T	-	-	-	ns
t(lc)	Clock low	12S requirement: min < 0.35 T	-	-	-	ns
t(sr)	Setup time	12S requirement: min < 0.2 T	15.6	-	-	ns
t(htr)	Hold time	12S requirement: min < 0	0	-	-	ns

3.8.3 Interintegrated circuit (I2C)

Table 3-18 Supported I2C standards and exceptions

Applicable standards	Feature exceptions	WCD9311 variations
I2C Specification, version 2.1, January 2000		None

3.8.4 Digital MIC PDM interface



Select (Sel)	Mode	Internal Signal
Vs	Right (Data1)	DMIC 1
GND	Left (Data2)	DMIC 2
Vs	Right (Data3)	DMIC 3
GND	Left (Data4)	DMIC 4
Vs	Right (Data5)	DMIC 5
GND	Left (Data6)	DMIC 6

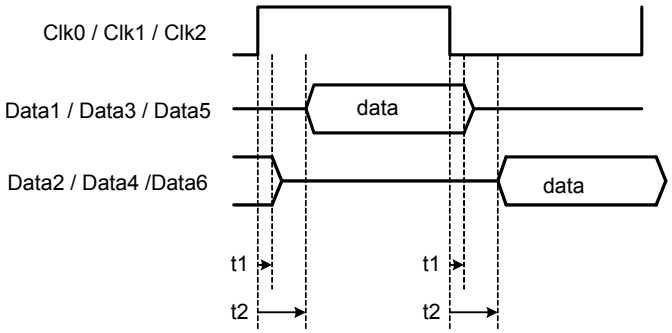


Figure 3-15 WCD9311 received clock signal constraints

Table 3-19 Digital microphone timing

Parameter	Comments	Min	Typ	Max	Units
T1		5	15	25	ns
T2		20	35	50	ns

3.9 Support circuits – analog

3.9.1 Microphone bias

Table 3-20 Microphone bias performance

Parameter	Comments	Min	Typ	Max	Units
Output voltage					
Normal operation	3 mA microphone load	1.70	–	2.85	V
MBHC calibration	No noise filtering in this mode	0.20	–	1.50	V
Output current	Two microphone loads of 1 to 1.5 mA each	–	–	3.0	mA
Microphone bias current consumption		–	80	150	µA
Output switch to ground					
On resistance		–	–	20	Ω
Sink current		2.0	–	–	mA
Output noise	0.1 µF bypass	0.5	2.0	3.0	µVrms
Power supply rejection ratio	100 mVpp applied to VDD_VBATT input				
at 20 Hz		93	–	–	dB
200 Hz to 1 kHz		113	–	–	dB
at 5 kHz		100	–	–	dB
at 10 kHz		90	–	–	dB
at 20 kHz		78	–	–	dB
Intermicrophone isolation	DC current = 50 µA, 2.2 kΩ bias resistor; 20 Hz to 80 kHz	70	–	–	dB
Noise filtering cap at CFILT pin		–	0.1	–	µF
Load capacitance					
With load cap mode		0	0.1	0.5	µF
No external cap mode		–	–	270	pF

3.9.2 Analog input through AUX_PGA

Performance of the following Tx path is specified in Table 3-21: analog input – AUX_PGA – power amplifier output.

Table 3-21 Analog input to AUX_PGA to output PA specifications

Parameter	Comments	Min	Typ	Max	Units
AUX PGA end to end					
SNR	Differential, gain = 0 dB, A-weighted Input = 1.02 kHz, -60 dBV				
Ear amp		101.0	104.0	–	dB
HPH amp		100.0	103.0	–	dB
Line amp		97.0	100.0	–	dB
THD + N ratio	Input = 1.02 kHz -13 dBv SE, gain = 12 dB				
Ear amp	Differential	80.0	–	–	
HPH amp	Single-ended	80.0	–	–	dB
Line amp	Single-ended	80.0	–	–	dB
Max. input voltage	f = 1.02 kHz				
Differential		0.94	1.00	1.06	Vrms
Single-ended		0.47	0.50	0.53	Vrms
Gain error	Input = 1.02 kHz, 0.5 dBv, differential	-0.5	–	0.5	dB
Frequency response	20 Hz to 20 kHz, input signal level = -20 dBv; applies to all paths, gain = 0 dB	-0.5	–	0.5	dB

3.10 Support circuits – digital

Digital logic characteristics are defined in Section 3.5; additional performance specifications are not required.

4 Mechanical Information

4.1 Device physical dimensions

The WCD9311 device is available in the 86 pin CSP that includes dedicated ground pins for improved grounding, mechanical strength, and thermal continuity. The 86 pin CSP has a 6.0 by 6.0 mm body with a maximum height of 1.27 mm. Pin A1 is located by an indicator mark on the top of the package. A simplified version of the 86 pin CSP outline drawing is shown in Figure 4-1.

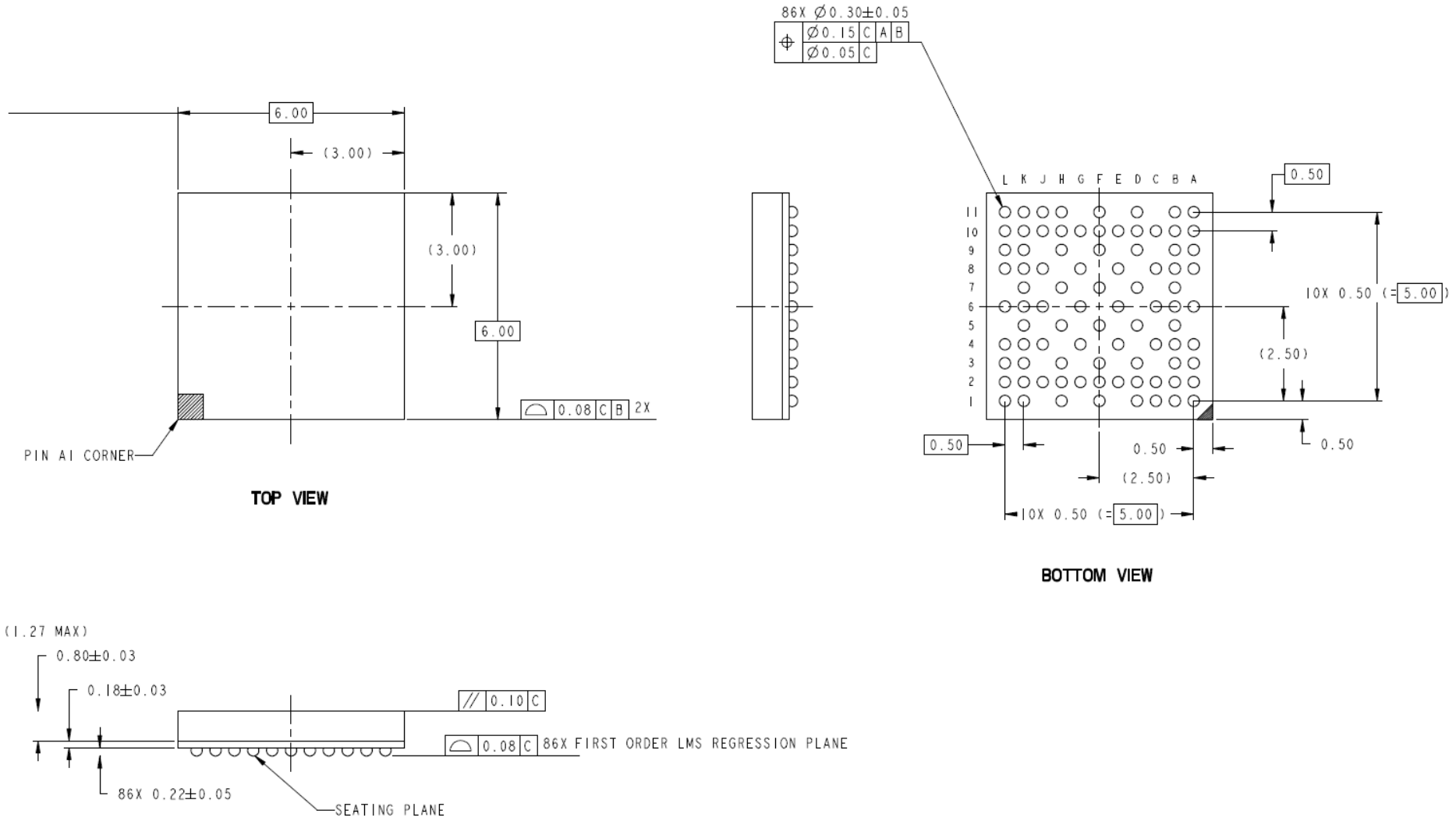


Figure 4-1 86 pin CSP (6.0 × 6.0 × 1.27 mm) outline drawing

4.2 Part marking

Figure 4-2 shows the package markings for the WCD9311 IC. Table 4-1 lists, line-by-line, the part markings for this device.

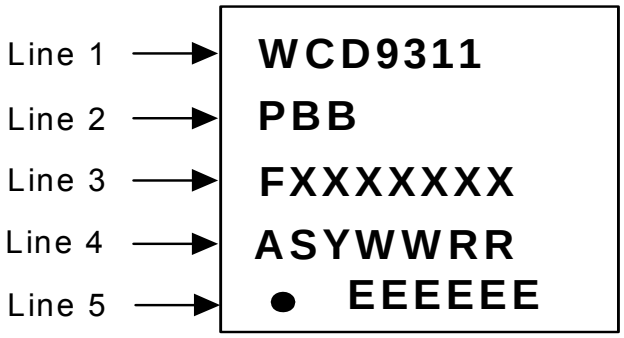


Figure 4-2 WCD9311 IC part marking (top view – not to scale)

Table 4-1 Part marking line descriptions

Line	Marking	Description
1	WCD9311	Product name
2	PBB	P = product configuration code (see Table 4-2) BB = feature code
3	FXXXXXXX	F = source of supply code XXXXXXX = wafer lot number
4	ASYWWRR	A = Fabrication: TSMC, Fab 12, Taiwan Y = single-digit year code WW = work week (based on calendar year) RR = product revision (see Table 4-2)
5	• EEEEEE	• = Pin A1 indicator EEEEEE = traceability number

4.3 Device ordering information

This device can be ordered using the identification code shown in Figure 4-3; the device ID code is explained in the following text.

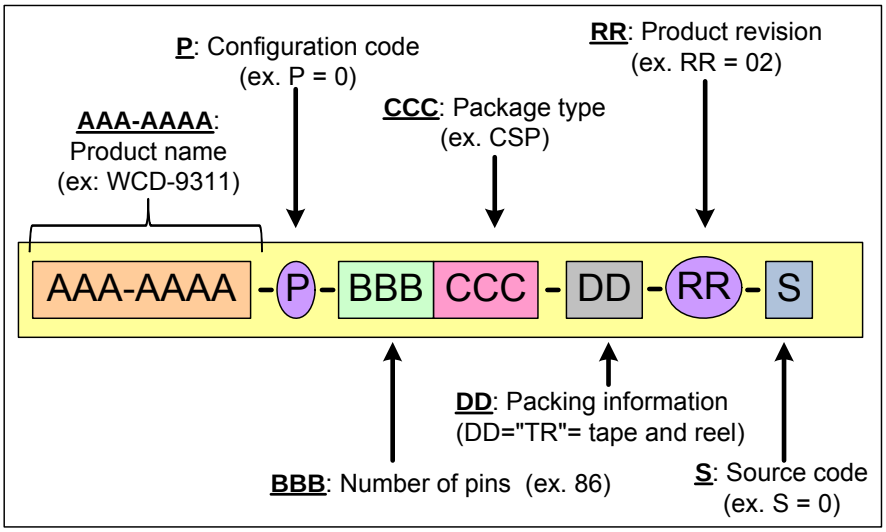


Figure 4-3 WDC9311 device identification code

An example for the WCD9311 device can be as follows: WCD9311-0-86CSP-TR-02-0.

Device ordering information details for all samples available to date are summarized in Table 4-2.

Table 4-2 Device identification code/ordering information details

PM variant	Product configuration code (*P*)	Product revision (*RR*)	HW ID #	S value [1]
ES1 sample type				
WCD9311	0	02	–	0

1. S is the source configuration code that identifies all the qualified die fabrication source combinations available at the time a particular sample type was shipped. S values are defined in Table 4-3.

Table 4-3 Source configuration code

S value	F value = A	F value = B	F value = C
0	TSMC	–	–

4.4 Device moisture-sensitivity level

The CSP devices are susceptible to damage induced by absorbed moisture and high temperature. The latest revision IPC/JEDEC J-STD-020 standard revision for moisture-sensitivity qualification is followed. ***WCD9311 devices are classified as MSL1@260ºC***. This is the MSL classification temperature, which is defined as the minimum temperature moisture-sensitivity testing during device qualification.

Additional MSL information is included in other sections of this document or in other documents:

- Section 5.2.1 – Storage
- Section 5.2.3 – Handling
- Section 7.1 – Reliability qualifications summary

4.5 Thermal characteristics

The WCD9311 device in its 86 pin CSP has the typical thermal resistance listed in Table 4-4.

Table 4-4 Device thermal resistance

Parameter		Comment	Typical	Units
θ_{JA}	Thermal resistance, J-to-A	Junction-to-ambient (still air) [1]	40	°C/W
θ_{JC}	Thermal resistance, J-to-C	Junction-to-case [2]	0.82	°C/W

1. Junction-to-ambient thermal resistance (θ_{JA}) is calculated based upon the maximum die junction temperature and the total package power dissipation; ambient temperature is 85°C.
2. Junction-to-case thermal resistance (θ_{JC}) applies to situations in which nearly all the heat flows out the top of the package.

5 Carrier, Storage, & Handling Information

Information about the shipping carrier and storing and handling the WCD9311 IC is presented in this chapter.

5.1 Carrier

5.1.1 Tape and reel information

The single-feed carrier tape for the WCD9311 device is shown in Figure 5-1, including its proper part orientation. The tape width is 16 mm and the parts are placed on the tape with a 8 mm pitch. The reels are 330.2 mm (13 inches) in diameter with 177.8 mm (7-inch) hubs. Each reel can contain up to 4000 devices.

The individual pocket design can vary from vendor to vendor. The pocket is designed to hold the part for shipping and loading onto SMT manufacturing equipment while protecting the body and terminals from damaging stresses. The 86-pin CSP devices are packaged in the tape and reel with the solder ball facing down.

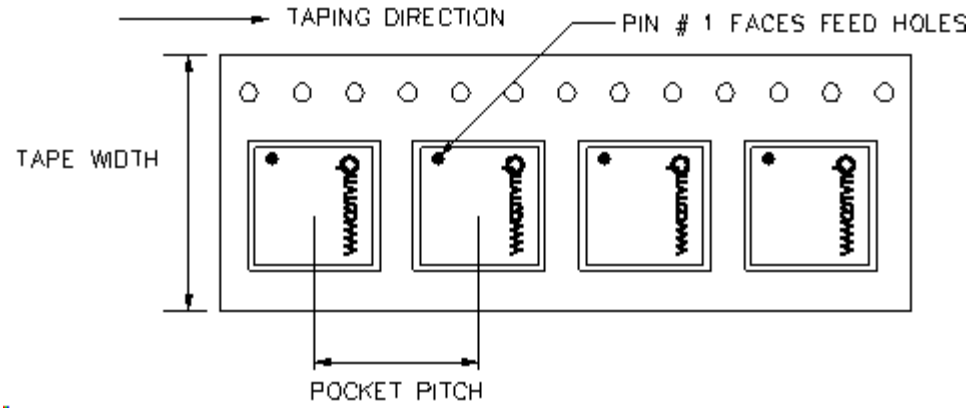


Figure 5-1 Carrier tape drawing with part orientation

The carrier tape and reel features conform to the EIA-481 standard:

- 8-mm through 200-mm embossed carrier taping
- 8-mm or 12-mm punched carrier taping of the surface mount components for automatic handling

Tape-handling recommendations are shown in Figure 5-2.

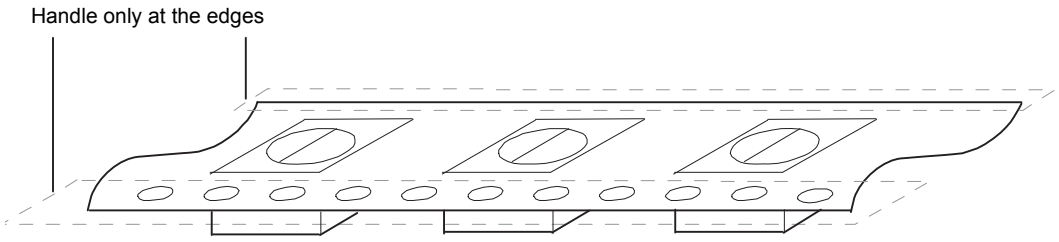


Figure 5-2 Tape handling

5.2 Storage

5.2.1 Storage conditions

WCD9311 devices, as delivered in tape and reel carriers, must be stored in sealed, moisture barrier anti-static bags. The calculated shelf life in a sealed moisture bag is 60 months; this value requires an ambient temperature lower than 40°C and relative humidity less than 90%.

It is recommended that these shipping and storage conditions for the CSP reel inside the sealed bag are followed:

1. Relative humidity between 15% and 70%
2. Temperature – room temperature lower than 30°C
3. Atmosphere – a nitrogen dry cabinet is highly preferred

5.2.2 Out-of-bag duration

The WCD9311 IC CSP has unlimited MET at < 30 C/85% RH.

NOTE The factory must provide an ambient temperature lower than 30°C and relative humidity less than 60%, as specified in the IPC/JEDEC J-STD-033 standard.

5.2.3 Handling

Tape handling was discussed in Section 5.1.1. Other handling guidelines include the following:

- Do not use hard-tip tweezers, as they may damage the CSP. Using a vacuum tip to handle the CSP is recommended.
- Carefully select the appropriate pickup tool to avoid any damage during the SMT process.
- Proceed with caution when reworking or tuning components that are in close proximity to the CSP.

5.2.4 Baking

It is **not necessary** to bake the WCD9311 devices.

5.2.5 Electrostatic discharge

Electrostatic discharge (ESD) occurs naturally in laboratory and factory environments. An established high-voltage potential is always at risk of discharging to a lower potential. If this discharge path is through a semiconductor device, destructive damage could result.

ESD countermeasures and handling methods must be developed and used to control the factory environment at each manufacturing site.

Products must be handled according to the ESD Association standard, ANSI/ESD S20.20-2007, *Protection of Electrical and Electronic Parts, Assemblies, and Equipment*.

Refer to Chapter 7 for the WCD9311 device ESD ratings.

6 PCB Mounting Guidelines

6.1 Land pad and stencil design

The land pattern and stencil recommendations presented in this section are based upon internal characterizations using lead-free solder pastes on an eight-layer test PCB, and a 100 micron-thick stencil. The PCB land pattern and stencil design for the 86 pin CSP is the same whether SnPb or lead-free solder is used.

6.2 SMT development and characterization

The information presented in this section describes board-level characterization process parameters. It is included to assist customers when starting their SMT process development; it is not intended as specifications for customer SMT processes.

NOTE It is recommended that customers follow their solder-paste vendor recommendations for the screen-printing process parameters and reflow profile conditions.

Characterization tests attempt to optimize the SMT process for the best board-level reliability possible. This is done by performing physical tests on evaluation boards. The tests may include the following:

- Peel test
- Bend-to-failure
- Bend cycle
- Tensile pull
- Drop shock
- Temperature cycling

It is recommended to characterize the land patterns according to each customer's processes, materials, equipment, stencil design, and reflow profile ***prior to PCB production***. Review the land pattern and stencil design recommendations in Section 6.1 as a guide for characterization.

Optimizing the solder stencil pattern design and print process is critical to ensuring print uniformity, decreasing voiding, and increasing board-level reliability.

Any particular underfill products are not endorsed.

Reflow profile conditions typically used for SnPb and lead-free systems are given in Table 6-1.

Table 6-1 Typical SMT reflow profile conditions (for reference only)

Profile stage	Description	Lead-free (high-temp) condition limits
Preheat	Initial ramp	< 3°C/sec max
Soak	Dry out and flux activation	150 to 190°C 60 to 120 sec
Reflow	Time above solder paste melting point	40 to 70 sec
	SMT peak package-body temperature	245°C
Cool down	Cool rate – ramp-to-ambient	6°C/sec max

6.3 SMT peak package-body temperature

Factory floor-life prior to solder-attach is addressed within Section 5.2.2 (Out-of-bag duration).

The following limits during the SMT board-level solder attach process are recommended:

- SMT peak package body temperature of 245°C – the temperature that must not be exceeded as measured on the package body's top surface
- Maximum duration of 40 to 70 seconds at this temperature

Although the solder paste manufacturer's recommendations for optimum temperature and duration for solder reflow must be followed, the recommended limits must not be exceeded.

6.4 SMT process verification

Verification of the SMT process prior to high-volume PCB fabrication is recommended, including:

- Electrical continuity
- X-ray inspection of the package installation for proper alignment, solder voids, solder balls, and solder bridging
- Visual inspection
- Cross-section inspection of solder joints to confirm registration, fillet shape, and print volume (insufficient, acceptable, or excessive)

7 Part Reliability

7.1 Reliability qualification summary

Table 7-1 Reliability evaluation summary

Tests, standards, and conditions	Sample Size	Result
Average failure rate (AFR) in FIT (λ) failure in billion device-hours: HTOL: JESD22-A108-A Use condition: temperature: Tj = 70°C, VDD nominal	569	30 FIT
Mean time to failure (MTTF) t = $1/\lambda$ in million hours	569	33 million hrs
ESD – human-body model (HBM) rating: JESD22-A114-D	3	2000 V
ESD – charge-device model (CDM) rating JESD22-C101-C	3	500 V
Latch-up (I-test): EIA/JESD78: Trigger current: ±100 mA; temperature: 85°C	6	Pass
Latch-up (Vsupply overvoltage): EIA/JESD78 Trigger voltage: 1.5 x Vnom V; temperature: 85°C	6	Pass
Moisture resistance test (MRT): J-STD-020 E Reflow at 260 +0/-5 °C	480	MSL 1
Temperature cycle: JESD22-A104-C Temperature: -55 to 125°C; number of cycles: 1000 Soak time at min/max temperature: 2 minutes Cycle rate: 2 cycles per hour (cph) Preconditioning: JESD22-A113-E MSL: 1, reflow temperature: 260 +0/-5°C	240	Pass
Unbiased highly accelerated stress test (UHAST): JESD22-A118-B Preconditioning: JESD22-A113-E MSL: 1, reflow temperature: 260 +0/-5°C	240	Pass
High temperature storage life: JESD22-A103-C Temperature 150°C, 1000 hours	90	Pass
Die shear: MIL-STD-883E, Method 2019	15	Pass
Solder ball shear: JESD22-B117	120	Pass
Solder bump shear	60	Pass

Table 7-1 Reliability evaluation summary (cont.)

Tests, standards, and conditions	Sample Size	Result
Flammability: UL-STD-94 NOTE: Flammability test – Not required (UL-STD-94) ICs are exempt from flammability requirements due to their sizes (per UL/EN 60950-1) as long as they are mounted on materials rated V-1 or better. Most PWBs onto which ICs are mounted are rated V-0 (better than V-1).	–	See note.
Physical dimension: JESD22-B100-A	60	Pass

A Terms and Acronyms

A1.1 Terms and acronyms

Table A1-1 defines terms and acronyms commonly used throughout this document.

Table A1-1 Terms and acronyms

Term	Definition
ADC	Analog-to-digital converter
ANC	Active noise cancellation
APQ	Application-only processor
bps	Bits per second
CDM	Charged-device model
CMOS	Complementary metal oxide semiconductor
CP	Charge pump
CSP	Chip-scale package
DAC	Digital-to-analog converter
DMIC	Digital microphone
DNC	Do not connect
DRE	Dynamic range enhancement
ESD	Electrostatic discharge
FM	Frequency modulation
HBM	Human-body model
HPH	Headphone
IC	Integrated circuit
I^2C	Inter-integrated circuit
I^2S	Inter-IC sound
I/O	Input/output
IIR	Infinite impulse response
kbps	Kilobits per second
LDO	Low dropout (linear regulator)
MBHC	Multibutton headset control
MIC	Microphone

Table A1-1 Terms and acronyms (cont.)

Term	Definition
MSBit or MSByte	Defines whether the MSB is the most significant bit or most significant byte. All instances of MSB used in this manual are assumed to be MSByte, unless otherwise specified.
NS	Nano second
OEM	Original equipment manufacturer
PA	Power amplifier
PCB	Printed circuit board
PCM	Pulse-coded modulation
PGA	Programmable gain amplifier
PM	Power management
RH	Relative humidity
RoHS	Restriction of hazardous substances
Rx	Receive, receiver
SE	Single-ended
SLIMbus	Serial low-power inter-chip media bus
SMT	Surface-mount technology
SNR	Signal-to-noise ratio
Tx	Transmit, transmitter
WCD	WSP coder/decoder
WSP	Wafer-scale package

B Exhibit 1

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