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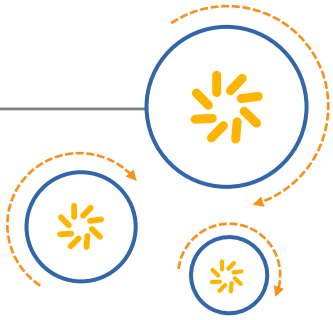

Qualcomm® Snapdragon™410E (APQ8016E) Processor

Device Revision Guide

LM80-P0436-69 Rev. A

May 24, 2017

For additional information or to submit technical questions, go to:

https://discuss.96boards.org/c/products/dragonboard410c

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Revision history

Revision	Date	Description
A	May 2017	Initial release

Contents

1 Introduction

This document contains a description of the chipset capabilities. Not all features are available, nor are all features supported in the software.

NOTE Enabling some features may require additional licensing fees.

Technical information for the APQ8016E device is primarily covered by the documents listed in Table 1-1. Released APQ8016E documents are posted here: https://discuss.96boards.org/c/products/dragonboard410c and are available for download.

Table 1-1 Primary APQ8016E documents

Document number	Document title
LM80-P0436-7	*Qualcomm Snapdragon 410E (APQ8016E) Processor Device Specification*
LM80-P0436-69 (this document)	*Qualcomm Snapdragon 410E (APQ8016E) Processor Device Revision Guide*

1.1 Acronyms, abbreviations, and terms

Table 1-1 provides definitions for the acronyms, abbreviations, and terms used in this document.

Table 1-1 Acronyms, abbreviations, and terms

Term	Definition
CS	Commercial samples
ES	Engineering samples
WCSS	Wireless connectivity subsystem
MMSS	Multimedia subsystem
PSS	Peripheral subsystem
AMSS	Advanced mobile subscriber station
JEDEC	Joint electron device engineering council
JTAG	Joint test action group
QTI	Qualcomm Technologies Inc
OEM	Original equipment manufacturer
PCB	Power control bus
SIMD	Single instruction multiple data

Table 1-1 Acronyms, abbreviations, and terms

Term	Definition
TAP	Test access port
MPM	Modem power manager
GPIO	General purpose input output
RPM	Remote power manager
NoC	Network on a chip
QDSS	Qualcomm debug subsystem
RAM	Random access memory
SSR	Smart status reports
WC	Wireless connectivity
FIFO	First-in-first-out

1.2 Scope and intended audience

This device revision guide identifies issues with all APQ8016E samples released to date. The following information is included:

- Introduction to this document and its topic (Chapter 1)
- Device identification (Chapter 2)
  - Device marking
  - Hardware revision number
  - Identification details for each sample type
  - Sample testing (ES and CS explanations)
  - Identification of compatible software releases
- Known issues (Chapter 2)
  - Issue description
  - Impact to system performance
  - Possible workarounds (what designers should do to minimize the issue's impact)

This device revision guide is intended for new product developers who are designing, testing, and/or evaluating phones or terminals that include the APQ8016E device.

1.3 Additional information

For additional information, go to:

https://developer.qualcomm.com/hardware/snapdragon-410/tools

2 Device identification

The APQ8016E device can be identified by markings on its top surface and by the contents of an identification register; these identification techniques are described in Section 2.1 and Section 2.2, respectively. Further details about each sample type are presented in Section 2.3 through Section 2.5.

2.1 Device marking

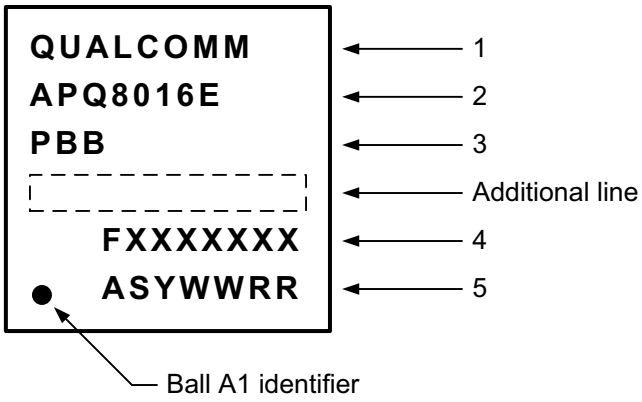

Figure 2-1 Device marking (top view, not to scale)

Table 2-1 Device marking line definitions

Line	Marking	Description
1	QUALCOMM	Qualcomm name or logo
2	APQ8016E	Qualcomm Technologies, Inc. (QTI) product name
3	PBB	P = product configuration code (see Table 2-3) BB = feature code (see Table 2-3)
	Blank or variable	Additional content as necessary
4	FXXXXXXX	F = supply source code ■ F = A (for GLOBALFOUNDRIES) ■ F = B (for TSMC) ■ F = C (for Samsung) XXXXXXX = traceability number

Table 2-1 Device marking line definitions (cont.)

Line	Marking	Description
5	ASYWWRR	A = assembly site code ■ A = U (Amkor, China) ■ A = K (SPIL, Taiwan) ■ A = V (JCET STATSChipPAC, China) ■ A = E (ASE, Taiwan) S = assembly sequence number Y = single/last digit of year WW = two-digit work week of year specified by Y RR = product revision (see Table 2-3)
	•	Pin 1 or pin A1 indicator
Additional lines may appear on the part marking for some samples; this is manufacturing information that is only relevant to QTI and QTI suppliers.		

2.2 Hardware revision number – general format

The device identification register allows the user to determine the device's manufacturer, part number, and version via the test access port (TAP). The 32-bit device identification register is read through the JTAG interface and is summarized in Table 2-2.

Table 2-2 Device identification register

Bit location	Description	Value
bits [31:28]	Version data (may change with sample type)	0x0
bits [27:12]	Part number (changes with sample type)	0x0706
bits [11:1]	Manufacturer identity code (administered by JEDEC)	0x0E (QTI's code)
bit [0]	Device identification register start bit	Always = 1

2.3 Device identification for each sample type

Table 2-3 provides details for identifying each sample type.

Table 2-3 Device identification details

Device	Product configuration code (*P*)	Product revision (*RR*)	HW revision number	Sample type	HW version	S value [1]	BB value [2]	Comments
APQ8016E	1	01	0x0 0706 0E1	ES/CS	2.0	0	VV	1.2 GHz ARM Cortex-A53 processor

1. S is the source configuration code that identifies all of the qualified die fabrication-source combinations available at the time a particular sample type was shipped. S values are defined in Table 2-4.
2. BB is the feature code that identifies an IC's specific feature set, which distinguishes it from other versions or variants. Feature sets are detailed in the Comments column.

NOTE Devices with date code (YWW) = 503 or later are CS devices.

Table 2-4 Source configuration codes

S value	Die	F value = A	F value = B	F value = C
0	Digital	GLOBALFOUNDRIES	TSMC	Samsung
Other columns and rows will be added in future revisions of this document, if needed.				

2.4 Sample testing

2.4.1 Engineering samples (ES)

These devices have undergone limited testing and sometimes have significant feature limitations. They are suitable to assist with PCB development, to conduct board-level electrical evaluation tests, and to explore manufacturing considerations. Engineering samples are not to be used for phone-level qualification.

2.4.2 Commercial samples (CS)

These devices have undergone full production-level testing and meet the specifications and features described in the device specification, except as otherwise noted in this document. They have passed device-level qualification. Commercial samples are suitable to be used for performance testing, and also phone-level production and qualification.

2.5 Compatible software releases

Each sample type is for use with a particular AMSS software release (or later). They are not expected to be compatible with AMSS software releases that occurred earlier than that particular revision. Table 2-5 identifies the software compatibility of each sample type.

Table 2-5 Software compatibility for each sample type (*PRR* value)

APQ device sample	PRR	Compatible software	Comments [1]
ES	x01	M8916AAAAANLYD1021 or later	
CS	x01	M8916AAAAANLYD1025 or later	

1. Refer to the corresponding software release notes for more details.

3 Known issues

3.1 Summary of known issues

All known issues for each revision of the APQ8016E device are summarized in Table 3-2. The text within the *Issue* column provides links to the sections of this document that explain the issues, regardless of the sample type (or types) on which they occur. An *X* in any of the other columns indicates that the issue occurs on the corresponding sample type.

The functional area categories are defined in Table 3-1.

Table 3-1 Functional area description

Functional area	Description
WCSS	Wireless connectivity subsystem
MMSS	Multimedia subsystem
A53	A53 processor subsystem
PSS	Peripheral subsystem
General	General area

Table 3-2 Known issues – all sample types and revisions[1]

#	Issue	Functional area [2]	APQ8016E CS
			All P variants
			RR = 01
			YWW ≥ 503 [3]
3-1	USB_ID connection issue	PSS	X
3-2	Jitter issue on MCLK signal	MMSS	X
3-3	Speculative data reads by Cortex-A53 might be performed to device memories	A53	X
3-4	NoC system bus deadlock during debugging	General	X
3-5	Wireless connectivity subsystem restart (SSR) fails	WCSS	X

1. P and RR values are detailed in Table 2-3
2. The functional areas are defined in Table 3-1.
3. Any device before this date has not undergone full production-level testing and does not meet the specifications and features described in the device specification. However, some parts, even with YWW < 503, are also CS parts. These parts are specially marked 503 in the additional line of device marking. Refer to the date code (YWW) and the additional line of device marking; see Section 1.2. Devices with date code (YWW) = 503 or later are CS devices. Devices with 503 in the additional line (default is blank) are also CS devices.

3.2 Issues – description, impact, and workaround

Issue 3-1 USB_ID connection issue

Description	The APQ8016E device does not support USB host mode if the USB_ID pin is used for host/peripheral detection during enumeration.
Impact	USB host mode is not supported with the USB_ID pin. Only the peripheral mode is supported.
Workaround	**Use GPIO_110 for USB cable insertion during sleep. Since the USB_ID pin is not used for detection, USB PHY will not be powered by VREG_L7 and VREG_L13 and can be turned off for lower leakage during standby.** To implement USB_ID functionality, OEMs can use any unused MPM wake-capable GPIO. If a GPIO other than GPIO_110 is used, the OEM is responsible for ensuring that the software change is implemented.

Return to Table 3-2

Issue 3-2 Jitter issue on MCLK signal

Description	Jitter on the camera MCLK has been observed at 24 MHz but not at frequencies less than 24 MHz.
Impact	Jitter on MCLK at 24 MHz may affect camera functionality.
Workaround	**The software workaround is to use a 23.88 MHz MCLK; however, this may reduce camera performance by 0.5% of the fps rate.**

Return to Table 3-2

Issue 3-3 Speculative data reads by Cortex-A53 might be performed to device memories

Description	ARM announced a new Cat A Erratum #829070 in Cortex-A53 that potentially affects all device memories that are susceptible to speculative reads. A load to a device memory, when done in the vicinity of advanced single instruction multiple data (SIMD) or floating point, can result in a speculative read to the device. This may cause a device to take action, based on speculative reads, that is not intended programmatically. For information, refer the link to A53 SDEN in ARM's information portal (requires registering on the ARM site): http://infocenter.arm.com/help/topic/com.arm.doc.subset.cortexa.a53/index.html
Impact	If any peripherals are mapped using device memory and have locations that have an impact on a read, then, these impacts could be observed for reads that were not requested by any load instructions executed by the processor.
Workaround	**The QTI default software does not result in the scenario that the erratum describes. However, if OEMs plan to add their own drivers/software to the default software for specific applications, they must ensure that the following conditions are met to avoid a scenario described in the erratum:** ■ **Advanced SIMD/VFP/Crypto instructions are not used in the kernel.** □ **Advanced SIMD/VFP/Crypto can still be used in a manner that does not lead to the scenario described in the erratum or with appropriate padding as indicated in ARM erratum statement. The OEM should evaluate whether there is any performance impact of this padding in their specific use case.** ■ **There is no device memory or strongly ordered memory mapping to user space.** □ **Device memory and strongly ordered refer to the memory attributes as defined in the *ARM Architecture Reference Manual* ARMv7-A.**

Return to Table 3-2

Issue 3-4 NoC system bus deadlock during debugging

Description	An NoC deadlock occurs in a corner-case concurrency scenario, when RPM is trying to access STM, and applications are in continuous burst transaction mode with peripherals.
Impact	Debugging through QDSS logging may not work in an extreme corner-case scenario. There is no impact on the functional mode of any application.
Workaround	**QTI's default software uses RPM message RAM for debugging purposes, which may not result in a deadlock issue. QTI recommends that OEMs use default software for debugging purposes.**

Return to Table 3-2

Issue 3-5 Wireless connectivity subsystem restart (SSR) fails

Description	When SSR is applied to the entire wireless connectivity (WC) block, a FIFO pointer does not get reset, which results in spurious transactions with memory devices, leading to functional failures of the WCSS.
Impact	A subsystem-level reset of the WCSS does not work. The WCSS has to be reset, block by block.
Workaround	**The software workaround is to ensure that the WLAN_XO is on (turn it on if it is off) and then to reset the WCSS blocks to fix this issue.**

Return to Table 3-2

EXHIBIT 1

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